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Tunnel Diode Digital Circuitry*

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Summary—This paper is divided into two parts. In the first part, ie basic tunnel diode logic circuits are discussed. These include the ionostable and the bistable analog-threshold gates and the "Goto-air," which uses the principle of majority decision. These circuits re studied to determine the requirement on tunnel diodes and other omponent tolerances. Relations between the "fan-in" and the fan-out" numbers and the component tolerances are derived. The sults indicate that the "Goto-pair" is somewhat superior to the nalog-threshold gates with respect to circuit reliability.

In the second part, a tunnel diode flip-flop stage which has ad-antages with respect to speed, ease, of operation and component lerances is described. Combination of these flip-flops in counter nd shift-register configurations have been successfully operated. everal potential advantages over conventional transistor circuits re discussed.

Introduction

SINCE the first publication concerning the tunnel diode by Esaki [1], a considerable amount of research and development effort has been directed owards the circuit application area as well as towards evice fabrication techniques. The enthusiasm which as developed for the tunnel diode has certainly not esulted simply because it is a two-terminal negative esistance device. Devices such as the four-layer diode, he unijunction transistor, the point contact transistor, he *p-n-p-n* hook transitor, and others also exhibit nega-ive resistance characteristics between one pair of their erminals. However, these devices have only received a noderate amount of attention. The advantages which nake the tunnel diode an important device arise be-ause of the quantum mechanical tunneling principle nvolved in producing the negative resistance charac-eristic. These include the potential of high-speed opera-ion, ruggedness with respect to environmental con-itions, and relative device simplicity.

In order to realize fully these potential advantages, he tunnel diode circuitry described in this paper con-ists only of tunnel diodes and common passive circuit omponents, such as resistors, capacitors and inductors. Other circuit elements, such as transistors, are pur-osely excluded from the basic circuit unit with the omplete understanding that under many circumstances he introduction of a two-port device would simplify he circuit.

The contents of this paper are divided into two parts. The first part describes various modes of tunnel diode ogic circuits and the requirements imposed upon the unnel diode characteristics with respect to the tol-rances of other circuit components. The second part lescribes a tunnel diode flip-flop circuit which has been ested with favorable results in certain applications.

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Basic Tunnel Diode Logic Circuits

The two obvious modes of operation are the monostable and the bistable conditions as shown in Fig. 1. The single stable point for the monostable case is represented by point a; and the two stable points for the bistable case are designated by points a and b, for the case when the bias resistance is large with respect to the negative resistance. They are a and b' if the bias resistance is moderate. The monostable logic circuits are shown in Fig. 2. The bistable logic circuits are shown in Fig. 3 and 4.

For all the circuits shown, the diode or diodes are at or near the stable point a just prior to a logic operation. Circuits shown in Figs. 2 and 3 use the analog-threshold principle where the analog sum of the input signals has to be equal to[1] or greater than the threshold level $(I_p - I_a)$ in order to give an output. The circuit shown in Fig. 4, which is known as the "Goto-pair," uses the principle of majority decision. The analog sum of the input signals should be of the correct polarity, and its amplitude should be larger than the difference between the two diode currents. After each logic operation, the diode (or diodes) of a bistable circuit must be reset to the stable point a in Fig. 1, either by using a negative pulse or by removing the bias supply temporarily.

The difficulty arising from the nonunilateral behavior of the above circuits can be overcome by using either the backward diode [3] or the rectifying diode to block the backward transmission or by using a three phase supply similar in principle to that described for digital circuits using parametric oscillators [2]. The logic stages are arranged in such a way that the backward flow of information does not affect the operation. Thus the interconnection of logic stages becomes straightforward. However, the allowable number of input circuits and the allowable number of output circuits are limited to a small value. They are related to the allowable tolerances of the circuit components.

Requirement on Tunnel Diode and Component Tolerances[2]

A. Analog-Threshold Logic

The monostable circuit shown in Fig. 2(a) can be studied together with the bistable circuit shown in Fig. 3(a) by assuming that the inductance L is reasonably

[1] Normally, a certain amount of overdrive is required to achieve high speed switching.

[2] In the following calculation a much simplified idealized diode characteristic is used. The amount of overdrive required for achieving high speed switching is not included. Therefore, the results are actually on the optimistic side.

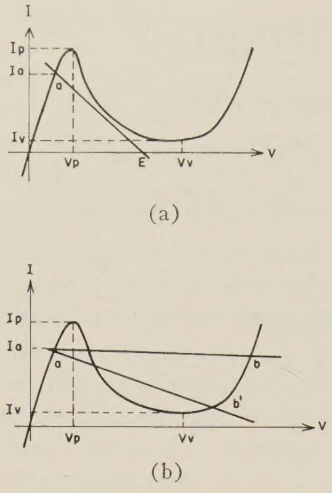


Fig. 1—Two modes of tunnel diode operation for digital applications. (a) Monostable bias condition. (b) Bistable bias condition.

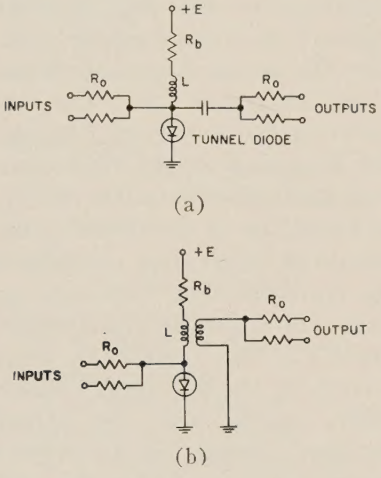


Fig. 2—Monostable logic circuits. (a) Change of diode voltage as the output. (b) Change of current as the output.

large so that during a large part of the output period this inductance behaves as a current source. Fig. 5 shows an idealized tunnel diode characteristic. A constant current load line intersects the V-I curve at points a and b. Referring to Fig. 3(a), let the number of input circuits be n, the number of output circuits be m, the nominal peak current of the diode be I_p, the valley current be I_v and the variation of these currents be $\pm k$ per cent. Let the variation of output voltage across the diode, the variation of resistors and supply voltage be $\pm \delta$ per cent. Each of the input currents representing a "1" is given by the output voltage divided by the resistor R_0. If the nominal value of each input current is I_{in}, for an AND gate of n inputs, the following conditions should be met at the input, for the transition from a to b,

$$nI_{in}\frac{(1-\delta)}{(1+\delta)} \geqq I_p(1+k) - I_a(1-\delta) \qquad (1)$$

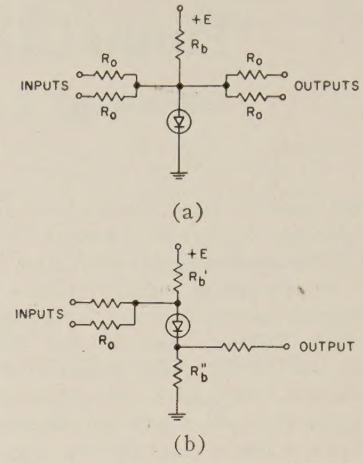


Fig. 3—Bistable circuits using analog-threshold logic. (a) R_b large, diode voltage as the output. (b) $(R_b'+R_b'')$ moderate, change of diode current as the output.

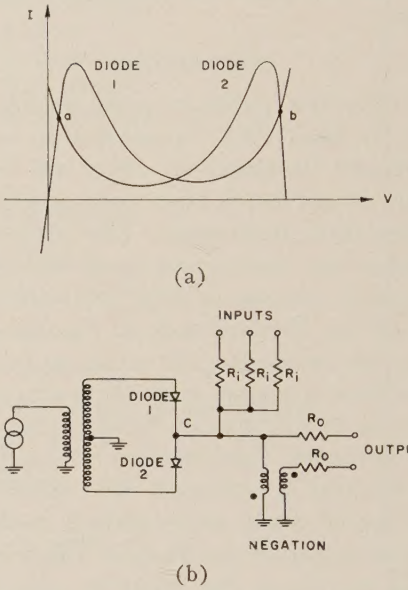


Fig. 4—Tunnel diode logic circuit using majority decision.

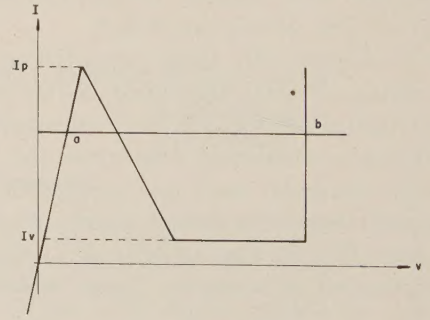


Fig. 5—Idealized tunnel diode characteristic for calculation of tolerances.

and, for staying at a, neglecting the very small amount of current representing "0,"

$$(n-1)I_{in}\frac{(1+\delta)}{(1-\delta)} \leqq I_p(1-k) - I_a(1+\delta). \qquad (2)$$

At the output of the preceding stage, the maximum available output current during switching is

$$I_b - I_v = I_a - I_v.$$

If no nonlinear device, such as a backward diode [3] or a rectifying diode is used in the input circuit to block the backward flow of information, each output circuit will have

$$I_0 = \frac{I_a(1-\delta) - I_v(1+k)}{m+n}. \tag{3}$$

If nonlinear devices are used to block the backward flow of current, then each output circuit will have

$$I_0' = \frac{I_a(1-\delta) - I_v(1+k)}{m}. \tag{3a}$$

The current I_0 or I_0' is equal to I_{in} in (1) and (2).

Taking the limiting case and combining (1) and (2) gives

$$\frac{I_{in}}{I_p} = \frac{2(k+\delta)}{1-\delta(2n-1)}. \tag{4}$$

Eq. (4) indicates the minimum value of each input current necessary for n inputs. Combining (3) and (4), since

$$I_a = I_p - \frac{(2n-1)}{2} I_{in}$$

gives

$$m+n = \frac{[1-(2n-1)(k+2\delta)](1-\delta) - \frac{I_v}{I_p}(1+k)[1-\delta(2n-1)]}{2(k+\delta)}. \tag{5}$$

Using (3a) instead of (3) leads to

$$m = \frac{[1-(2n-1)(k+2\delta)](1-\delta) - \frac{I_v}{I_p}(1+k)[1-\delta(2n-1)]}{2(k+\delta)}. \tag{5a}$$

Eq. (5a) shows the advantage of using a nonlinear device to block the backward flow of information. As an example, if $I_p/I_v = 10$, the relationship between the tolerances on the diode currents and the tolerances on the other components is shown in Fig. 6 for the case given by (5).

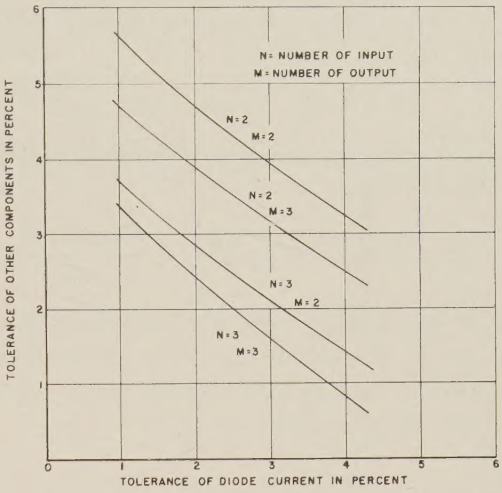


Fig. 6—Relation of tolerances and "fan-in" and "fan-out" numbers.

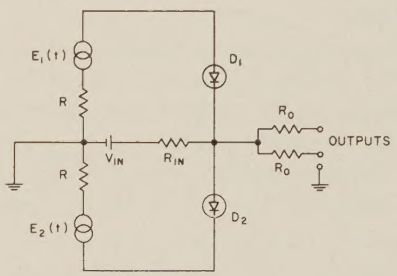


Fig. 7—An equivalent circuit of a "Goto-pair" prior to the switching of one of two diodes.

B. *Majority Logic*

The tolerance for the circuit components shown in Fig. 4 is calculated as follows; Fig. 7 shows an equivalent circuit. The input circuit is represented by a small voltage V_{in} in series with R_{in}. V_{in} is the equivalent voltage which produces the desired input current. The value of R_{in} depends upon the number of input circuits. Resistance R represents the internal resistance of the supplies E_1 and E_2. These two supply voltages may be slightly unbalanced in amplitude and in phase if an ac voltage is used. Let the total combined unbalance be represented by a tolerance of voltage $\pm\delta$ per cent; the variation of resistance R_o be $\pm\delta$ per cent; and the variation of diode currents be $\pm k$ per cent.

Let the number of input circuit be $(2n-1)$ and the number of output circuit be m, where n is a positive integer. Let the nominal value of each input current

be I. Under the worst condition, the resultant of the inputs will be

$$I_{in} = I[1 - 2(2n - 1)\delta]. \tag{6}$$

If the supply voltage is sinusoidal, at the time when one of the diodes switches

$$I[1 - 2(2n - 1)\delta] \geqq 2kI_p + \frac{mE2\delta \sin\theta}{R_0} \tag{7}$$

where E is the nominal peak value of the supply. The value of E has to be such that only one of the diodes can be switched to the high-voltage low-current state at any time. Thus

$$E(1 + \delta) < [I_p(1 - k) - I_2']\left[R + \frac{R_0}{m + (2n - 1)}\right] + I_2'R, \tag{8}$$

where I_1' and I_2' are the currents in diodes D_1 and D_2 respectively. Eq. (8) specifies the peak amplitude of the supply voltage.

In the three phase supply scheme described in the literature, the information from one stage is transmitted to the following stage within a 60° overlapping period. After passing the information to the following stage, the supply voltage becomes too small for the information to be retained. Letting ϕ be the resetting angle gives

$$2E \sin\phi = V_v + 2RI_v + R\frac{E(1 + \delta)\sin\phi - RI_v}{R + \dfrac{R_0}{m + (2n - 1)}} \tag{9}$$

where V_v and I_v are the voltage and current at the valley point respectively. Eq. (9) gives the relationship between the angle of resetting and the input and the output numbers.

As an approximation, the voltage drop across R in the above equations may be neglected and θ and ϕ assumed to be approximately 30° and 150°, respectively. Combining (8) and (9) and taking the limiting case leads to

$$V_v(1 + \delta) = [I_p(1 - k) - I_2']\frac{R_0}{m + (2n - 1)}. \tag{10}$$

The total output current is given by

$$I_{out-total} \cong [V_v(1 + \delta)\sin\phi] \Big/ \frac{R_0}{m + (2n - 1)}$$
$$= \sin\phi[I_p(1 - k) - I_2']. \tag{11}$$

Letting

$$I_p(1 - k) - I_2' = xI_p, \tag{12}$$

since

$$I = \frac{I_{out-total}}{m + (2n - 1)}$$

and by combining (7) and (11) gives

$$\delta \cong \frac{1 - \dfrac{2k[m + (2n - 1)]}{x \sin\phi}}{2(2n - 1)}. \tag{13}$$

It is desirable to keep x as close to unity as possible. However, the limit of x is determined by $(1 - I_v/I_p)$. Fig. 8 shows the relationship between the tolerance of the diode and the tolerance of other circuit components for $\phi = 150°$, $x = 0.8$, and $(2n - 1) = 3$.

It is clear that, when the diodes of each stage are selected for matched currents, the allowable tolerance of the other circuit components becomes reasonable.

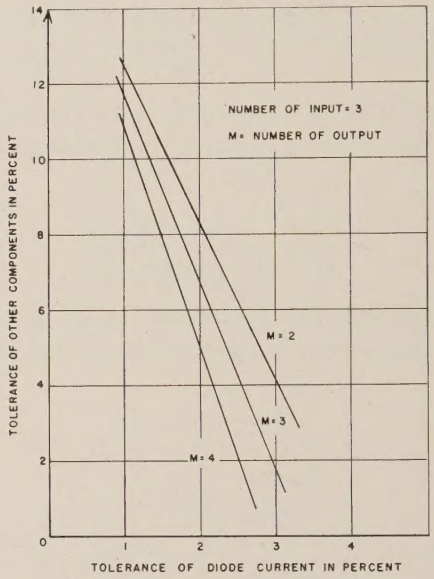
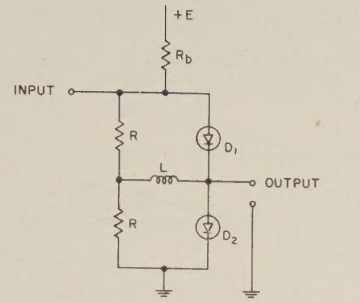


Fig. 8—Relation between the tolerance of diode current and the tolerance of other components.

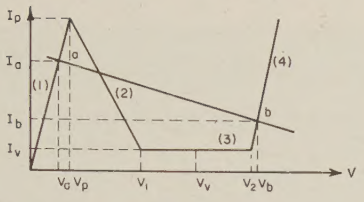
Sequential Logic Circuit

Sequential logic circuits, such as flip-flops and counters, can be constructed by interconnecting the basic logic stages shown in Fig. 2–4 using the three-phase supply scheme. The basic principle involved has been described in articles on digital circuits using parametric subharmonic oscillators [2]. This type of sequential circuits often consists of four or more basic logic stages with each sequential operation taking the time of a complete rotation of the three-phase supply.

Fig. 9 shows a tunnel diode flip-flop circuit which performs in the same manner as a center-triggered transistor flip-flop stage. The input triggering pulse is connected across two diodes to ground. The output is taken as the voltage across diode D_2. The principle of operation is as follows. The dc supply is of such a magnitude that only one of the two diodes can be in the high-voltage, low-current stage; the other diode has to be in the low-voltage, high-current state. The difference between the two diode currents flows through the inductance and returns to the supply. Under steady-state conditions there is no voltage drop across



(a)



(b)

Fig. 9—A tunnel diode flip-flop circuit. (a) A tunnel diode flip-flop circuit. (b) Idealized diode characteristics and the steady-state bias condition.

the inductance. When an input pulse triggers the OFF diode to ON (low-voltage, high-current to high-voltage, low-current), a voltage is induced across the inductance which resets the other diode from ON to OFF. Thus each pair of positive input pulses completes a switching cycle.

The circuit shown in Fig. 9(a) can be studied as follows: Referring to Fig. 9(b), under steady-state conditions, the bias points of diodes D_1 and D_2 are assumed to be at points b and a respectively. The V-I curve of the diode is idealized into four line sections as shown. The fourth section which represents the high-voltage region is assumed to have a slope equal to that of the first section. The slope of the second section is determined by the negative resistance of the tunnel diode. The third line section represents the region where the diode current is practically equal to the valley current I_v. The valley voltage V_v is assumed to be approximately equal to the arithmetic mean of V_1 and V_2. If the negative resistance of the diode is $(-r)$,

$$\begin{aligned} V_1 &= V_p + r(I_p - I_v), \\ V_2 &= 2V_v - [V_p + r(I_p - I_v)], \\ V_a &= \frac{V_p}{I_p} I_a, \end{aligned} \tag{14}$$

and

$$V_b = V_2 + \frac{V_p}{I_p}(I_b - I_v).$$

The difference between the diode currents, $(I_a - I_b)$ flows through inductance L and resistor R.

Referring to Fig. 9(a), the supply voltage E has to be at least large enough to let one of the diodes pass its peak current point; but not large enough to support both diodes at the valley point (V_v, I_v), or one diode at the valley point and one diode at the peak point (V_p, I_p). Thus

$$\left[\left(\frac{V_p}{R}+I_p\right)R_b+2V_p\right] < E < \left[2V_v+\left(I_v+\frac{V_v}{R}\right)R_b\right]$$

$$\text{or} \quad \left[V_v+V_p+\left(I_p+\frac{V_p}{R}\right)R_b\right], \tag{15}$$

whichever is smaller. The following equations also have to be satisfied:

$$(I_a - I_b)R = V_b - \frac{V_p}{I_p} I_a \tag{16}$$

and

$$E = R_b\left(I_a + \frac{V_a}{R}\right) + V_a + V_b. \tag{17}$$

The value of inductance L is determined in the calculation of the switching transient. Since the circuit components R, L, and the diode capacitance are the important factors in the switching transient, the value of R, calculated by using the above equations, should be checked for switching transients.

Fig. 10 shows the equivalent circuit used for transient calculation. Figs. 11–13 show the effect of L, R and the diode capacitance on the rise and fall time of the flip-flop.

The triggering pulse required can be estimated using the equivalent circuit shown in Fig. 14. The path provided by the inductance is neglected. Thus, for a step current pulse having an amplitude I:

$$V_p - V_a = \frac{IR_0R_2}{R_0R_1R_2C^2}\left[A + Be^{-at} + De^{-bt}\right], \tag{18}$$

where

$$A = \frac{1}{ab},$$

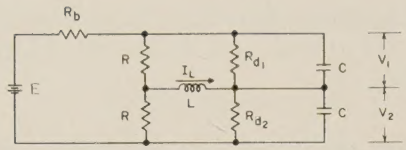
$$B = \frac{1 - CR_1a}{a(a - b)},$$

$$D = \frac{CR_1b - 1}{b(a - b)},$$

$$a = \frac{1}{2}\left[\frac{R_0(R_1 + R_2) + 2R_1R_2}{R_0R_1R_2C}\right] + \sqrt{\left[\frac{R_0(R_1 + R_2) + 2R_1R_2}{2R_0R_1R_2C}\right]^2 - \frac{R_0 + R_1 + R_2}{R_0R_1R_2C^2}},$$

$$b = \frac{1}{2}\left[\frac{R_0(R_1 + R_2) + 2R_1R_2}{R_0R_1R_2C}\right] - \sqrt{\left[\frac{R_0(R_1 + R_2) + 2R_1R_2}{2R_0R_1R_2C}\right]^2 - \frac{R_0 + R_1 + R_2}{R_0R_1R_2C^2}},$$

$$R_0 = \frac{2R_bR}{R_b + 2R},$$



For $t=0$ The initial conditions

$$I_L = I_a - I_b$$
$$V_1 = V_b$$
$$V_2 = V_p$$
$$R_{d_1} = \frac{V_b}{I_b}$$
$$R_{d_2} = \frac{V_v}{I_v}$$

For $t=\tau$ at which

$$V(\tau) = V_v$$
$$I_L = I_L(\tau)$$
$$V_2 = V_2(\tau$$
$$R_{d_1} = \frac{V_a}{I_a}$$
$$R_{d_2} = \frac{V_b}{I_b}$$

Fig. 10—The equivalent circuit and initial conditions for transient calculations.

R_1, R_2 represent the equivalent resistances presented by the diodes. As an example, for a circuit having

$R_b = 300$ ohms $\qquad R_2 = 50$ ohms

$R = 560$ ohms $\qquad C = 20$ $\mu\mu$f

$R_1 = 3000$ ohms $\qquad V_p - V_a = 15$ mv.

The required trigger pulse is $I=0.5$ ma peak with a duration longer than 3 mμsec.

The maximum output current is determined by the difference $(I_p - I_v - V_v/R)$ under steady-state conditions. However, if the inductance is large, under the transient conditions, the output current can be approximately $(I_p - I_v)$ for a large portion of the ON cycle.

Several flip-flop stages can be interconnected to form a counter as shown in Fig. 15. Fig. 16 shows the output waveform of this two-stage counter, operating with an input pulse rate of 3 mc. A four-stage counter was built in a similar manner for measuring the propagation delay from input to output. The total delay was 160 mμsec or 40 mμsec per stage. This amount of delay per stage corresponds to the rise time of the output of each stage tested. Nonbinary scalers can be constructed with proper feedback loops following a principle similar to the one used for transistor circuits.

Fig. 17 shows the circuit of a shift register using the flip-flop as the building block. Both the signal pulses and the shift pulses are positive. The shift pulse always switches the lower tunnel diode from "0" to "1" (from low-voltage, high-current to high-voltage, low-current), and the signal pulse switches the upper diode from "0" to "1." If a signal pulse switches the upper diode from

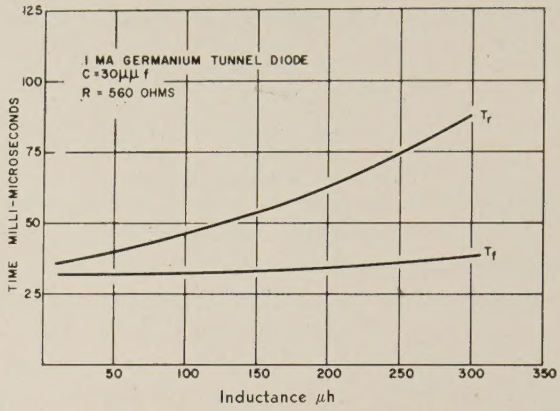


Fig. 11—Effect of inductance on the rise and fall time.

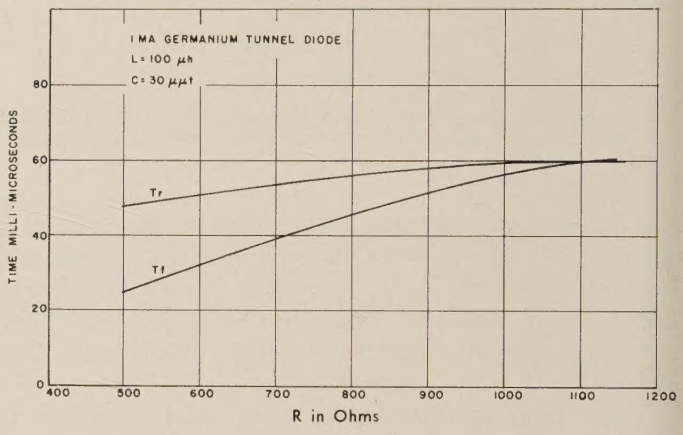


Fig. 12—Effect of resistance R on the rise and fall time.

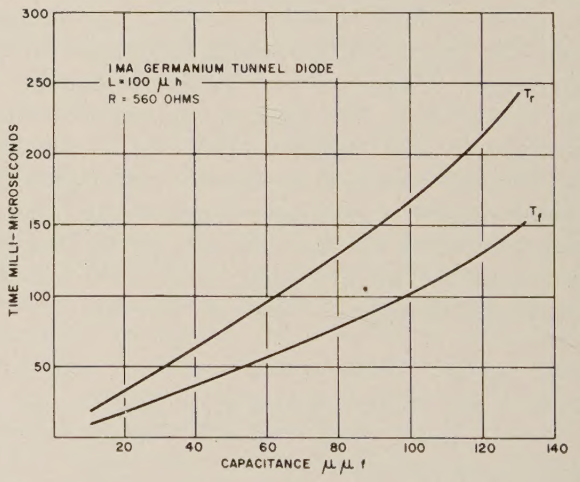


Fig. 13—Effect of junction capacitance on the rise and fall time.

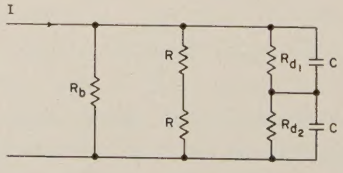


Fig. 14—Equivalent circuit for calculating the trigger pulse.

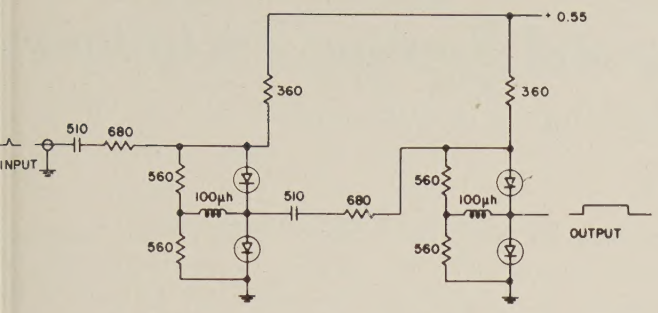
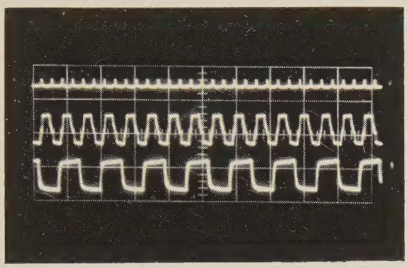
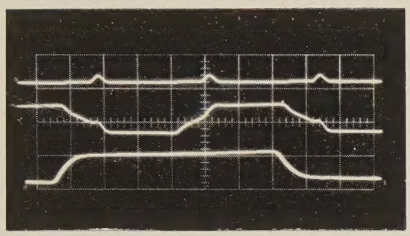


Fig. 15—Cascading of two flip-flops.



(a)



(b)

Fig. 16—3-mc pulse countdown by four using tunnel diode scaler (100 μh inductance). (a) 0.5 volt per division vertically, 1 μsec/division horizontally (time axis from right to left). (b) 0.5 volt per division vertically, 0.1 μsec/division horizontally (time axis from right to left).

0" to "1," the lower diode is reset from "1" to "0," the utput being a negative pulse which does not affect the llowing stage. When the shift pulse switches the lower iode from "0" to "1," a positive output pulse is obained. This output is delayed a period equal to or reater than the rise time of the flip-flop but less than he period of the clock or shift pulse. The delayed pulse witches the upper diode of the following stage from "0" o "1," and thus the information is shifted from left to ght.

The basic flip-flop circuit has been designed and ested to operate reliably for a tolerance of diode peak urrent variation of ± 5 per cent, a tolerance of resistnce of ± 5 per cent, and dc supply variation of ± 12 er cent.

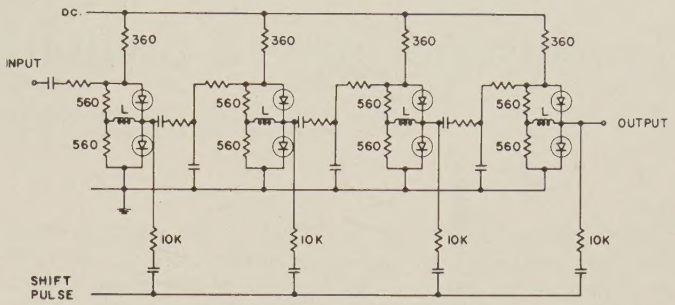


Fig. 17—Shift register.

Conclusions

Among the basic tunnel diode logic circuits described above, the two diode circuit which is known as the "Goto-pair" appears promising if the two diodes are carefully selected for matched currents. However, unless both diodes have essentially identical V-I characteristics (and ac characteristics for high-speed switching) with respect to all environmental conditions, a slight change in the environment, such as the temperature, may upset the circuit operation. The selection of diodes does not appear to be a practical proposition.

The flip-flop circuit described has the distinct advantage of simplicity over a transistor flip-flop of comparable speed. This tunnel diode circuit appears to be useful for certain applications such as counters and registers.

The severe tolerance requirements inherent in the discussed tunnel diode logic circuits certainly should not be considered as indicative of the future. It is the author's belief based on work going on in the Electronics Laboratory and elsewhere that with the improvement of tunnel diode fabrication techniques and the accumulation of knowledge concerning circuit behavior, practical tunnel diode logic circuits will be produced.

Acknowledgment

The author wishes to thank B. H. Rutter, J. Sterling, and D. L. Berry for their assistance in making the many measurements.

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[1] L. Esaki, "New phenomenon in narrow germanium *p-n* junction," *Phys. Rev.*, vol. 109, p. 603–604; January 15, 1958.
[2] E. Goto, "The parametron, a digital computing element which utilizes parametric oscillation," Proc. IRE, vol. 47, pp. 1304–1316; August, 1959.
[3] I. A. Lesk, N. Holonyak, Jr., U. S. Davidsohn, and M. W. Aarons, "Germanium and silicon tunnel diodes design, operation and application," 1959 WESCON Convention Record, pt. 3, pp. 9–31.
[4] M. H. Lewin, "Negative-resistance elements as digital computer components," *Proc. EJCC*, pp. 15–27; December, 1959.

Transistor Current Switching and Routing Techniques*

D. B. JARVIS†, L. P. MORGAN†, AND J. A. WEAVER†

Summary—A system of circuit logic is described in which transistors, particularly diffused base transistors, are operated well out of saturation in order to make the most of their speed. Logical information is contained in the presence or absence of a current which can be switched or routed by the gates described. Also described is the application of this system of logic to certain specific computer problems, namely, a parallel adder with a carry propagation time of 40 mμsec over 6 stages, a shifting register capable of operating at 10 mc and a binary decoder with a maximum delay of 40 mμsec.

I. Introduction

SOME of the new transistors produced by diffusion processes only have high-speed switching characteristics when operated well out of the saturation region. This paper describes circuits in which these transistors may be used.

The base-to-collector current gain of a transistor varies both with time for a given transistor and from transistor to transistor within a given type so that a known base current will not give a known collector current. The collector current must be fairly well defined in order to keep within the transistor ratings and normally, if the transistor bottoms, this is achieved by having a defined collector load. If the transistor is not to bottom, however, the current must be defined in the emitter circuit. For high-speed working, it is desirable to minimize delays caused by stray capacitance by making all voltage swings as small as is allowed by other circuit considerations. The long-tailed pair circuit allows a defined current to be switched with a small voltage signal and the circuits described herein are based on this circuit.

The information signal from the gates is a current from the collector of a transistor but the input to a gate is in the form of a voltage swing. One elegant solution to this problem has been described by Yourke[1,2] and used both *p-n-p* and *n-p-n* transistors in complementary circuitry. But for various economic and technical reasons, both types of transistor with similar characteristics are not always available. Other methods must be used if the circuits can only use one type of transistor. The usual resistance chain with capacitive speed-up can be used as the coupling element, but as the collector-to-base voltage of the transistor must always be greater than several volts, the coupling tends to be rather inefficient or involves pattern sensitivity because of the large voltage translation. A better scheme, described in Section II, uses a Zener diode as a coupling element. But this coupling is very sensitive to component tolerances and so is inefficient if economic or reliability considerations demand allowance for large tolerances. If several voltage supplies are allowed, it is possible to couple the inputs and outputs of gates (Section II) directly. There is a limit to the number of voltage supplies which can be used, and so a compromise system of circuit logic can be devised which involves both the latter two types of interconnection; such a system is described in Section II. In certain cases with this system, advantages both in speed and economy may be obtained over the more straightforward system using only one voltage supply and Zener diode connection. The cost is in slightly more complicated design rules. Certain computer units have been constructed for a specific project using the ideas introduced in Section II and are described in Sections III–V. They are a parallel adder, a shifting register and a binary decoder, respectively.

II. Current Switching and Routing

Fig. 1(a) shows a current switching gate as suggested by Yourke.[1,2] Current I_1 flows from one or the other of the two outputs, depending on the voltages on the two bases A and B, and the output currents are converted into base signals with the circuit shown in Fig. 1(b). When the input current is zero, current I_4 equals 3 ma. When the input current is 6 ma, I_4 equals 3 ma, but in the reverse direction. The corresponding voltage signal produced across the resistor R_1 is suitable for driving transistor bases such as A and B. A Zener diode has very suitable characteristics for use in this way. Its approximate equivalent circuit is shown in Fig. 2. The slope resistance R is typically only a few ohms so that the potential difference between the terminals of the diode remains essentially constant even though the current through it may change. The junction capacitance C is typically only 100 pF so that the RC time constant is sufficiently short to allow repetition rates of tens of megacycles a second.

The switching current I_4 is given by the algebraic addition of the two larger currents I_2 and I_3 as well as the signal current, so that small fractional variations in these produce large fractional variations in I_4.

* Received by the PGEC, February 23, 1960.

† Mullard Res. Labs., Salfords, Eng.

[1] H. S. Yourke, "Millimicrosecond transistor current switching circuits," IRE Trans. on Circuit Theory, vol. CT-4, pp. 236–240; September, 1957.

[2] H. S. Yourke and E. J. Slobodzinski, "Millimicrosecond transistor current switching techniques," *Proc. WJCC*, pp. 68–72; February, 1957.

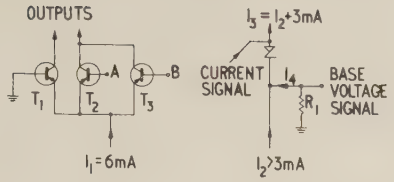


Fig. 1—Current switching system.

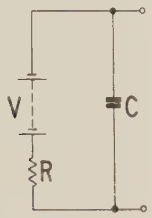


Fig. 2—Approximate equivalent circuit of a Zener diode when operating in the Zener breakdown region.

Therefore, if the coupling is to be efficient in the worst case, the resistors and voltages, which define I_2 and I_3 in practice, must have low tolerances and the voltage defining I_3 must be sufficiently great to make negligible the tolerance on the diode Zener breakdown voltage which increases the power dissipated in the associated resistor.

It is possible, however, to connect these gates simply if more than one voltage rail is allowed, as Fig. 3 shows. Gates 1 and 2 are similar to those previously described, and the output current signal from gate 1 is used to drive the base of T_1 in gate 3. Current I_4 is now determined by the comparable current I_3 and the signal only, and is therefore less susceptible to component tolerances. The common emitter current of a gate now may be a logic signal as it is in gate 3, which is a two-input AND gate. Throughout this paper, the convention is that the presence of a current represents a logical "1" and the absence of current a logical "0." The time delay for an input current change to propagate to the output is smaller for the emitter input than for the base input; as in the former case, there are only base transit time delays. But there is no gating threshold at the emitter and complementary outputs are not generally available. The signal is only restandardized when a constant emitter current is switched.

The EXCLUSIVE-OR gate is particularly simple in the current routing system. Two versions are shown in Fig. 4. In the circuit of Fig. 4(a), two current routing AND gates have been combined to make the EXCLUSIVE-OR gate. The high-impedance output of the transistors allows them to be merely commoned to form an OR gate. This is generally an acceptable procedure only if there will never be more than one unit of current from the junction, as is obviously the case with this gate. If the complementary output is sacrificed, the

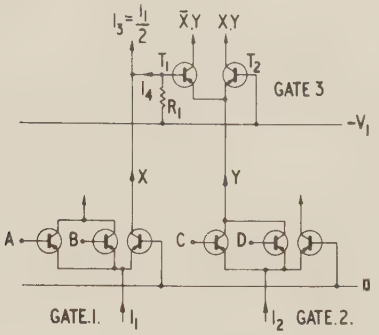
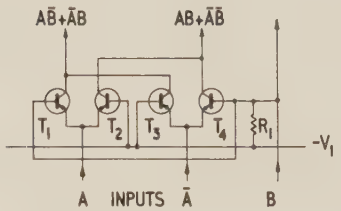
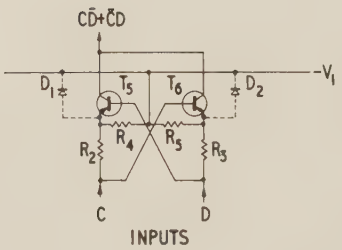


Fig. 3—An example of current routing.



(a)



(b)

Fig. 4—Two EXCLUSIVE-OR gates.

EXCLUSIVE-OR gate can be converted into a half-adder. The currents from T_1 and T_3 together give the partial sum signal and the current from T_2 alone gives the partial carry signal. Fig. 4(b) shows the circuit of another EXCLUSIVE-OR gate which uses fewer transistors.[3] The operation is as follows. With no current at C or D, both transistors T_5 and T_6 are cut off. If there is a current at C and not D, T_5 conducts with a base path of R_3 and R_2 and, similarly, if there is a current at D and not C, T_6 conducts. If, however, there is a current at both inputs, both transistors are cut off by the potentials developed across R_2 and R_3 and there is no output current. The circuit speed is increased and its susceptibility to component tolerances decreased if the voltage excursion of the transistor emitters is limited either with silicon diodes D_1 and D_2 as shown dotted, or with germanium diodes returned to a voltage slightly more positive than $-V_1$. This circuit forms the basis of the binary half-adder described in Section III.

[3] L. P. Morgan and J. A. Weaver, British Patent Application 25876/58.

III. High-Speed Parallel Adder

A. Description of Adder Stages[4]

The complete circuit diagram of one stage of the parallel adder is shown in Fig. 5. It consists of two half-adders. Inputs X and Y, representing the two binary digits to be added, are in the form of currents from a high-impedance source. A current of 8 ma represents a "1" and no current represents a "0."

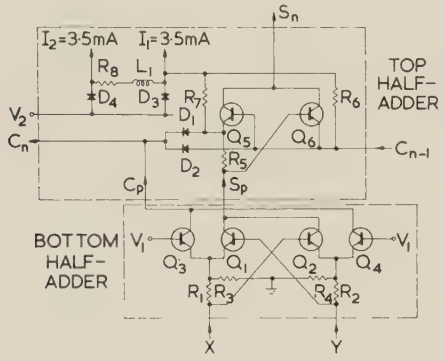


Fig. 5—One stage of the parallel adder.

Consider the bottom half-adder. When there is no current input at X and Y, there can be no partial sum current S_p or partial carry current C_p as all transistors are cut off. If there is a current at X but not at Y, transistor T_2 is cut off by the voltage developed across R_1, and T_1 conducts with a base current through both R_2 and R_4. T_3 cannot conduct because of the reverse bias V_1. Similarly, when there is a current at Y but not at X, transistor T_2 conducts. The high output impedance of the transistor allows the collectors to be merely joined together to form an OR function. When there is a current at X and Y, both T_1 and T_2 are cut off and the common emitter potentials of T_1, T_3 and T_2, T_4 increase positively until transistors T_3 and T_4 conduct to give a current output C_p. R_3 and R_4 are in parallel with the emitters of T_3 and T_4, and, with V_1, are so chosen that only one unit of current (8 ma) flows out as the partial carry C_p, even though two units of current flow into the half-adder at X and Y. Also, because R_3 is in parallel with the emitter of T_1, S_p is slightly less than 8 ma (about 7 ma).

Consider now the top half-adder. It is similar to the bottom half-adder, except that transistors equivalent to T_3 and T_4 are replaced by diodes D_1 and D_2 so that the carry current can flow directly into the following stage without going through a voltage level changing unit. The diodes are biased in the reverse direction by making the voltage V_2 about 0.6 volt more positive in each successive stage. If there is a current at S_p and not at C_{n-1}, T_5 conducts and T_6 is cut off. Similarly, T_6 conducts when there is only a current at C_{n-1}. The currents are slightly attenuated by R_6 and R_7, so that the sum output current S_n may be as low as 5 ma. When there is a current at S_p and C_{n-1}, both transistors T_5 and T_6 are cut off and diodes D_1 and D_2 conduct. Under these conditions, T_6 is cut off by the potential developed across R_5, but T_5 is cut off only by the difference in forward voltage of the conducting diodes D_1 and D_2. Depending on the diodes used, it may be necessary to use an extra resistor in series with D_1 to insure that T_5 is cut off. Again, although the input to the half-adder is two units of current, in order not to overload successive stages, only one must be propagated; so it is arranged that one unit of current is lost through R_6 and R_7.

When the carry current is propagated over several stages, the potential of the whole top half-adder increases positively and so, if the carry current is still to be well defined, R_6 and R_7 must be returned to current sources I_1 and I_2 as shown in Fig. 5. Imagine first of all that the inductance L and R_8 are shorted out. Then R_6 and R_7 are connected to a low-impedance current source I_1+I_2 which equals the partial sum current (approximately 7 ma). Therefore, not more than 7 ma can be lost from the top half-adder and 8 ma is propagated. The inductance speeds up the transients by making the extra current I_2 available for charging stray capacities. R_8 improves the recovery of the inductance.

As the voltage V_2 must increase positively with each successive stage, it is found that there is a limit of about six to the number of stages which can be directly cascaded. Between every six stages of the adder there must be a level changing unit.

Consider the condition when there is a partial carry current generated in the first of m stages of the adder and a partial sum in the other $m-1$ stages. The carry signal is then propagated over the $m-1$ stages and the $m-1$ pairs of diodes D_1 and D_2 conduct. Therefore, if the transistors T_3 and T_4 in the first stage are not to bottom, the diode of the mth stage must be connected to a low-impedance point of potential sufficiently negative to allow for the forward voltage V_F of the carry diode. Therefore, the voltage V_2 of the first stage is approximately:

$$-m(V_F + 0.6 \text{ volt}).$$

There is a limit to this voltage, however, which is set by the allowable power dissipation in the transistors. The worst case occurs when a partial sum current is produced in the bottom half-adder of the first stage and absorbed in the top half-adder of the same stage; the collector voltage of T_1 and T_2 is then approximately equal to V_2 and the collector current about 7 ma. It will be realized also that the greater the number of stages over which the carry signal is propagated, the greater are the voltage swings of the top half-adders and so the

[4] L. P. Morgan and J. A. Weaver, British Patent Application 26505/58.

carry current delay is not a linear function of the number of stages of propagation. Therefore, a reasonable limit to the number of stages directly cascaded is when an extra stage increases the maximum delay by more than would a level changing unit.

The limit set by both these considerations is about six stages.

B. Level Changing Unit

This unit involves the use of a switching pair T_8 and T_9 with T_7 acting as a low- to high-impedance buffer stage (Fig. 6).

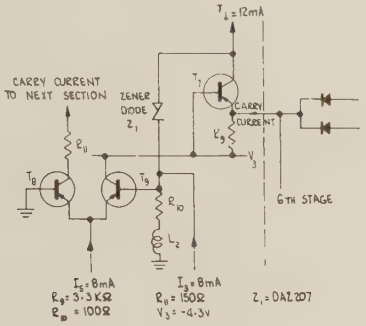


Fig. 6—Level changing unit using OC44 transistors.

When there is no carry current, the base of T_9 is held negative with respect to earth by a net current of 4 ma flowing through R_{10}. But when there is a carry current of 8 ma, there is a net current of 4 ma in the reverse direction through R_{10}, T_9 is cut off, and I_5 flows through T_8. R_{11} is used to avoid unnecessary power dissipation in T_8.

The current sources for the whole adder were obtained by connecting the appropriate value of resistor to either -120 volts or $+13.5$ volts, but the former voltage could be considerably reduced without much loss in performance.

C. A Carry Skip Technique

The time which must be allowed for each addition in a parallel adder of the type described, in which there is no provision for detecting when the carry signal has finished propagating, is equal to the longest addition time. Therefore, as most of this addition time is carry propagation time, it would be useful to reduce the latter. A carry skip technique has been used with the adder which reduces the maximum addition time by a factor of 2 without much extra circuitry.

Consider a section of m stages of the adder. It will be seen that if at least one digit input to each stage in the section is a "1" and there is a carry input of "1" to the section, there will be a carry output of "1" from the section. Now circuitry can be added to determine whether a carry input of "1" would give rise to a carry output of "1" in which case it generates a carry input of "1" directly to the next section. If the time taken for the inspection of the inputs and generation of the carry current is less than the time taken for the carry signal to propagate through the stages of the section, a saving of time is obtained. Fig. 7 shows the logical circuitry that gives this facility. Although this circuitry will ensure that a "1" is propagated more quickly, it may not insure that a "0" will propagate more quickly; actually, this is the case with the adder described, but it will be shown in Section III-D that this can easily be overcome.

It can be shown, theoretically, that this skip technique is most efficient when the number of stages in a section is made a variable with respect to the position of the section in the complete adder. But in this case, where the number of stages which can be directly cascaded is limited, it is not possible to obtain this maximum efficiency. However, the efficiency obtained is not much less than this maximum.

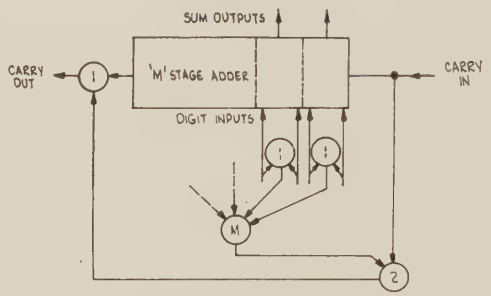


Fig. 7—Logical diagram for the carry skip technique.

D. Application of the Carry Skip Technique[5]

The modification to each stage is shown in Fig. 8. One extra transistor and three point contact diodes are required. Fig. 9 shows the modified level changing unit. Only 3 extra transistors and a resistor are required.

The line AB in Fig. 8 connects all the emitters of the 6 transistors T_{10} in a section to transistor T_{12} at C (Fig. 9). The base of T_{12} is at V_1 so that if the base of any of the 6 transistors T_{10} is held more negative than V_1, the current I_6 cannot flow through T_{12}. Now consider one stage. If there is an input current at X, diode D_6 conducts current I_7 and the base of T_{10} is caused to be at a voltage more positive than V_1. Similarly, the base voltage is positive if there is a current only at Y or at both X and Y. The current source I_7 limits the amount of current which can be lost from the input lines and has a value determined by the peak base current of T_{10} when switching. Therefore, when there is at least one input of "1" to each stage, the current I_6 flows through T_{12}.

[5] L. P. Morgan and D. B. Jarvis, British Patent Application 42063/58.

Consider now the skip unit (Fig. 9). The bases of T_9 and T_{10} are connected so that the collector current of T_{12} can be routed according to the carry input signal to the section. The collector of T_{11} is connected to the emitter of T_7 of the next level changing unit. Therefore, if the conditions for skipping are fulfilled, a carry input current to the emitter of T_7 of one level changing unit causes two units of current to flow into the emitter of T_7 in the next level changing unit. One unit of current is the skip current which arrives from T_{11} directly and the other is the carry current which has propagated through the 6 stages of the section. Now that it is possible to get two units of current flowing into T_7, the currents I_3 and I_4 in Fig. 6 must be changed to currents I_8 and I_9 in Fig. 9 if T_7 is to be kept out of bottoming. R_{12} produces a relatively low-impedance base path for T_{10} when a current is routed through T_{12} and T_{10}.

Whenever the inputs to the adder are changed, the carry skip facility described will insure that a carry current of "1" is propagated quickly, but it will not break down as quickly a carry current path that is already established; this being equivalent to propagating a carry signal of "0." If, however, all carry current paths are broken for a short time while the input currents are changing, by turning off I_5 in every level changing unit, only the shorter propagation time need be allowed for in the addition time.

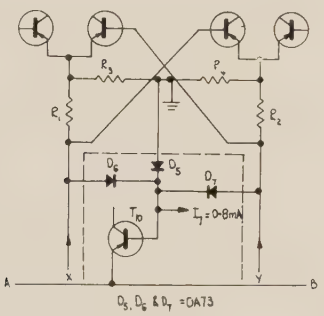


Fig. 8—Modifications to each stage of the adder.

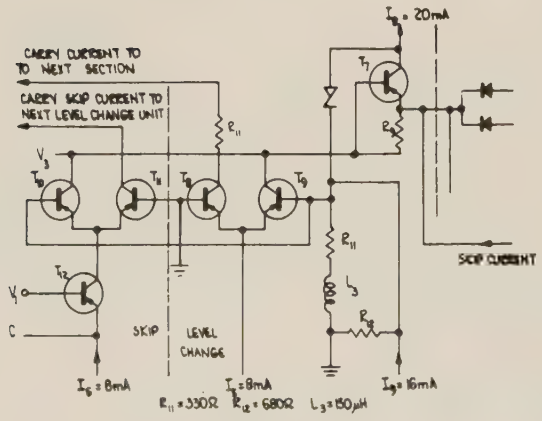


Fig. 9—Level changing and skip unit.

E. Performance

A 52-stage adder consisting of 8 sections of 6 stages and a final section of 4 stages has been constructed to this design using OC44 transistors and the performance was checked by using interrupted dc inputs. It was found that the carry propagation delay over a section was about 200 mμsec and the delay in skipping about 60 mμsec so that the maximum carry propagation time was about 750 mμsec. It was assumed that there would be adequate time for changing the inputs and strobing the outputs within 1 μsec.

The delay through a level changing unit is about the same as through a skip unit. It is interesting to estimate that without the skip facility, the addition time would be about 2 μsec.

As the appropriate pulse inputs have not yet been available, the propagation time of a carry "0" has not been observed.

The transistors mainly limit the speed of operation of the adder and so it would be expected that a version using OC170 transistors would be about 5 times faster, and this has been confirmed by obtaining a carry propagation time over 6 stages of 40 mμsec.

IV. A Shifting Register

Fig. 10 shows one stage of a 6-stage shifting register that has been built using OC170 transistors. It has facilities for shifting the binary information to the left and to the right in the register and for inverting the digit in each stage. The design can be simply modified, however, to shift the information in any desired way.

Transistors T_1 and T_2 are a current routing pair, but interconnected to give a bistable circuit, which will be recognized as a normal emitter coupled bistable. The transistors are kept out of bottoming and so a certain stabilizing factor is lost. Therefore, to insure long-term reliability, 5 per cent high-stability resistors must be used for the cross-coupling and base bias networks.

Transistors T_3 and T_4 are also a current routing pair and route the trigger pulses to the bistable. If the base of either T_1 or T_2 is made more positive by passing a current through T_4 or T_3, then the defined current I_1 flows in either T_2 or T_1, respectively. No regeneration in the bistable is necessary if the trigger current is large enough. Therefore, if a trigger current is applied to the common emitter of T_3 and T_4, the bistable will be set into a state defined by the voltage on the base of T_4. Diode D_2 is merely a catching diode to prevent T_4 bottoming.

Current i_1 is the output from the register for direct coupling to the adder described in Section III. The bistable is defined to be in a state "1" when $i_1 = 8$ ma and a state "0" when $i_1 = 0$. The current i_2 in the other side of the bistable is used to give information about its state to the shifting circuitry.

When the bases of T_5, T_6, and T_7 are positive with respect to earth, current i_2 merely flows through D_1,

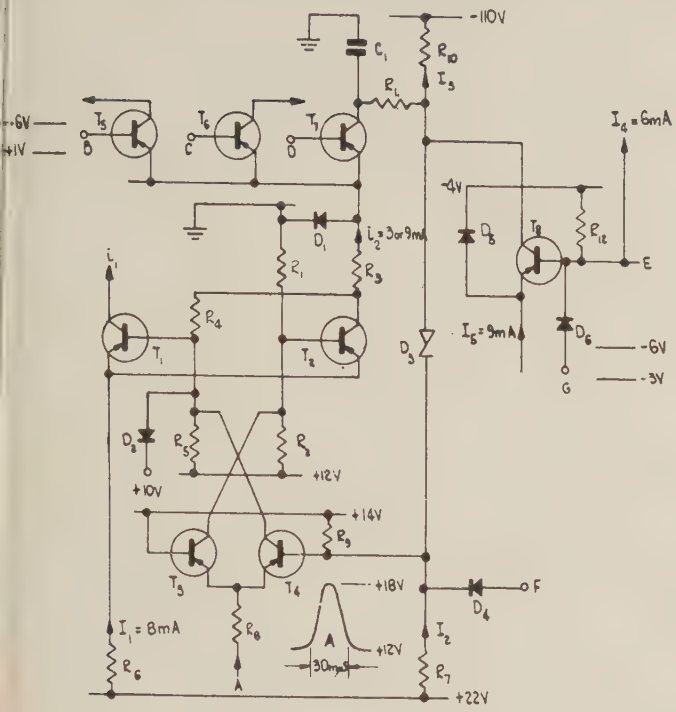


Fig. 10—One stage of the shifting register.

but if the base of any one of these transistors is made negative, that transistor conducts the current i_2. The information contained in i_2 can, therefore, be routed to any one of a number of paths and the number of paths is not limited by the bistable circuitry. The bistable must, of course, be designed so that the change in voltage to which R_3 is connected does not affect the stability of the two states.

So that the adder output could be used directly to set a register, the collectors of T_3 and T_4 are connected such that when the base of T_4 is positive with respect to V_2, a "1" is set in the bistable. If i_2 is allowed to flow through T_7 and then into the voltage translating unit D_3, a "0" in the bistable will set the base of T_4 so that the next trigger pulse at A will set a "1." Therefore, a negative voltage at D and a trigger pulse cause the digit in the stage to be inverted.

Other voltage sources may be used to set a "1" into the register by using diodes (*e.g.*, D_4).

Transistor T_8 and diode D_5 act as an inverter. Normally, an inhibit voltage is applied at G so that I_5 cannot flow through T_8, but when the inverter is required, the collector current of T_8 is controlled by a current applied at E.

For a shift right facility, the collector of T_6 is connected to the point E of the next stage to the right. Similarly, for a shift left facility, the collector of T_5 is connected to the point E of the next stage to the left.

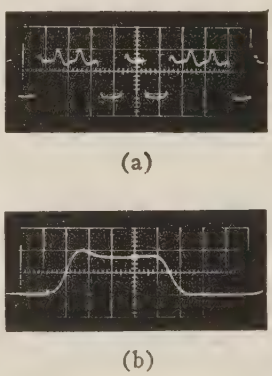
If the bistable is to trigger reliably, there must be adequate delay between a change in i_2 in the bistable and the corresponding change in voltage of the base of a transistor T_4. It was found that there was adequate delay when the inverter T_8 was used, but when the current i_2 passed through only one transistor (*e.g.*, T_7), it was necessary to use extra capacitive delay, C_1.

It was found that the register could be used with any of its three facilities when a trigger pulse was applied every 100 mμsec. The output current rise times are better than 20 mμsec, as can be seen in Fig. 11. Fig. 11(a) shows the output of one stage of the register when a pattern of 111010 is recirculated by continually shifting to the right and allowing the sixth stage to shift into the first. Fig. 11(b) shows part of this on a faster timebase in order to show the edges.

V. All Transistor Binary Decoder

An elegant example of the use of current routing is in a binary decoder. The principle of the method is shown in Fig. 12. A_2, A_1, A_0 represent a 3-digit binary number, A_2 being the most significant digit. As before, a more positive voltage signal (corresponding to the presence of a current from a *p-n-p* transistor) represents a logical "1." It will be seen that each "level" of switching is controlled by the corresponding digit. For example, if the word to be decoded is 101, the current I flows through the transistors marked S to output 5. Further levels with corresponding branching can be added to decode bigger numbers.

A 5-binary-digit decoder with 32 outputs has been constructed using OC170 transistors. It was found that the maximum delay between input and output was about 40 mμsec and that the system would transmit a



(a)

(b)

Fig. 11—(a) Horizontal: 100 mμsec/division; vertical: 2 volts per division. Output of one stage of the register when shifting pattern 111010 (voltage across 390Ω). (b) Horizontal: 20 mμsec/division. Vertical: 2 volts per division. Single "1" output magnified. Oscilloscope amplifier rise time equals 12 mμsec.

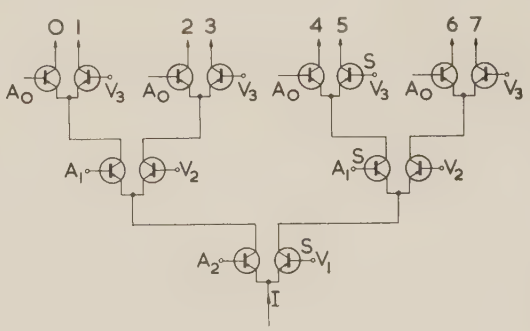


Fig. 12—Three-digit binary decoder.

current rise time of about 20 mμsec. It was necessary to current amplify the A_0 digit signal with a switching pair before it was used to switch the final level of transistors because of the high capacitive load represented by 16 reverse biased base emitter junctions. With some combinations of input digits, spurious breakthrough pulses can appear at the outputs, and especially the 0 output, but these only occur in the 40 mμsec of delay time, so are unlikely to be an embarrassment.

VI. Conclusions

A system of current routing circuit logic and its application to several computer problems has been described. A 52-stage parallel binary adder and a 4-stage shifting register have been constructed using OC44 transistors. An addition takes about 1 μsec and a shift can be accomplished every 0.5 μsec. Using OC170 transistors, a 6-stage parallel adder with a carry propagation time of 40 mμsec and a shifting register capable of shifting every 100 mμsec have also been built. Again, using OC170 transistors, a 5-digit binary decoder gave a maximum delay of 40 mμsec and was capable of propagating a 20-mμsec current edge without much degradation. Although the circuits given have not been fully developed, the experimental results obtained show that this system of logic makes the most of the speed of a given transistor while still allowing noncritical and economic circuits.

The speed of these circuits is limited primarily by the cutoff frequency of the transistors used and higher speed will be obtained by simply substituting higher-frequency transistors.

VII. Appendix

The OC44 is an alloy junction transistor intended for use in RF circuits. Some typical characteristics are:

$$\left.\begin{aligned} f_\alpha &= 15\text{ mc} \\ R_{bb'} &= 110\Omega \\ C_c &= 10\text{ pF} \end{aligned}\right\} (V_c = -6\text{ volts}, I_e = 1\text{ ma})$$

$$V_{c(pk)}\text{ maximum} = -15\text{ volts}$$

$$I_{c(pk)}\text{ maximum} = 10\text{ ma}$$

$$I_{co} = 0.5\,\mu\text{a}\ (V_c = -2\text{ volts}, 25°\text{C})$$

$$P = 43\text{ mw}\ (45°\text{C})$$

The OC170 is an alloy-diffused transistor intended for use in RF circuits. Some typical characteristics are:

$$f_1 = 70\text{ mc}$$

$$C_c = 2\text{ pf}$$

$$V_{c(pk)}\text{ maximum} = -20\text{ volts}$$

$$I_{c(pk)}\text{ maximum} = 10\text{ ma}$$

$$I_{co} = 2.0\,\mu\text{a}\ (V_c = -6\text{ volts}, 25°\text{C})$$

$$P = 60\text{ mw}\ (45°\text{C})$$

As this transistor is intended for RF use, it may be necessary to select, for those with good reverse base, emitter characteristics for use in computing circuits.

Magnetic Film Memories, A Survey*

A. V. POHM†, member, ire, and E. N. MITCHELL‡

Summary—**An analysis is made of the modes of magnetization reversal and rotation in thin ferromagnetic films. The ways in which the various modes can be employed for destructive and nondestructive memories are discussed and their performance limitations considered. Existing film memory efforts are partially surveyed and the material and system problems are examined. Possible future developments are also discussed.**

I. Introduction

SINCE the modern work of Blois [1] in 1954, there has been an expanding interest in magnetic films and magnetic film memories [2–29]. This interest has developed partly from the attractive magnetic characteristic which some magnetic films possess and partly from the logical and construction flexibility which magnetic films offer in memory design. There are, however, material uniformity problems which are playing an important part in the commercial availability of these memories.

II. Magnetic Film Characteristics

Thin magnetic films for memory applications usually are characterized by a magnetically induced uniaxial axis of anisotropy (rest direction) in the plane of the film. This uniaxial axis of anisotropy is established typically by use of an "orienting" magnetic field during formation by vacuum deposition [1] or electrodeposition [12]. The uniaxial anisotropy can be modified or induced by other factors, such as the angle-of-incidence of

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e depositing metal vapor [28]. For materials such as 0 per cent Ni–20 per cent Fe permalloy, this uniaxial axis of anisotropy can also be established or modified by means of a magnetic anneal [10]. Depending upon the material, method of preparation, and peculiarities of the sample, the uniaxial anisotropy may vary over a considerable range.

For a large thin flat film, if the rotation of the saturation magnetization M (in gauss) in the plane of the film from rest position is measured by the angle ϕ, and the rotation out of plane of the film by the angle ψ, the uniaxial anisotropy energy is given by

$$E_A = K_1(\sin^2\phi\cos^2\psi + \sin^2\psi)$$

to a good approximation [4, 18], where K_1 is the anisotropy constant. The demagnetizing field normal (shape anisotropy) to the plane of the film ($4\pi M \sin\psi$) is normally much larger than the anisotropy field. Including the shape anisotropy, the total anisotropy energy is given by:

$$E = K_1(\sin^2\phi\cos^2\psi + \sin^2\psi) + \frac{4\pi M}{2}\sin^2\psi$$

$$= \frac{H_K M}{2}(\sin^2\phi\cos^2\psi + \sin^2\psi) + \frac{4\pi M}{2^4}\sin^2\psi.$$

The anisotropy field (H_K) is defined as the ratio $2K/M = M/X_0$, where X_0 is the initial susceptibility in the transverse direction with the magnetization in a remanent state.

The static and quasi-static magnetic characteristics of these films have been studied using hysteresis loop display apparatus operating at low frequency [1, 4, 5, 9] and by directly observing the domain structure of the film by means of the Kerr apparatus [6] or Bitter techniques [23]. As indicated in Fig. 1(a) and (b), the hysteresis loop when observed at low frequency (the order of 100 cps) is essentially rectangular when observed in the rest direction, and closed when observed in the transverse direction. As the relative thickness of the film is increased, the rest direction loop [Fig. 1(a)] typically changes from the form indicated by the dotted line to that indicated by the dashed line because of an increasing demagnetizing field. The solid loops in Fig. 1(a) and (b) are typical of permalloy as used in memory applications. The dotted loop shown in Fig. 1(b) would be typical of a film grown in the absence of an orienting field and this loop would be observed in any direction in the plane of the film. Fig. 1(c) and (d) represents typical domain patterns for a film in its remanent and demagnetized states. The number of domains in the demagnetized state may vary considerably, depending on the manner in which the film is demagnetized. In a typical 1-cm diameter film of permalloy, it is difficult to reduce the domain size so that individual domains cannot be distinguished by the naked eye.

Magnetization reversal in magnetic films can occur by three overlapping modes [1], domain wall movement [1, 2, 20], "nonuniform rotation" [16], and uniform rotation [3, 4]. The way in which a particular film undergoes magnetization reversal depends upon material properties and the experimental conditions during switching.

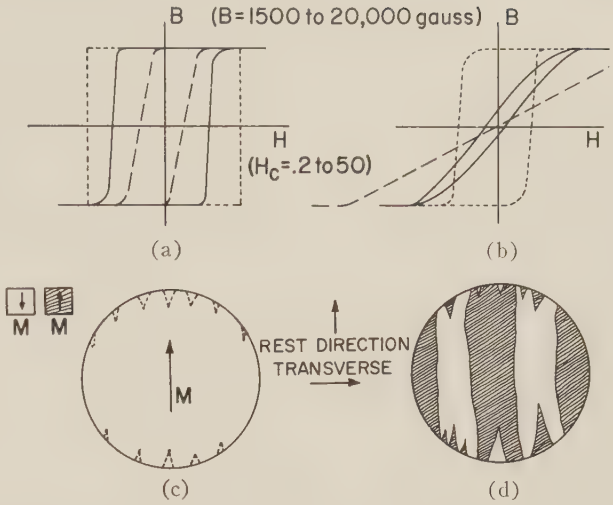


Fig. 1—"Typical" magnetic film hysteresis and domain characteristics. (a) "Typical" rest direction loops depending on thickness, material, shape, etc. (H in oersteds) (b) "Typical" transverse direction loops depending on anisotropy, material, shape, etc. (c) "Typical" remanent state domain pattern. (d) "Typical" demagnetized state domain pattern.

If the magnetization is reversed slowly, switching normally occurs by domain wall movement. The walls are usually of the Bloch or Ne'el type but sometimes possess a more complex structure. Fig. 1(d) illustrates domains of reverse magnetization and the domain boundaries. Upon slowly increasing the switching field, typically, the domain walls or boundaries can be observed to move. Materials such as certain permalloy samples may undergo extremely slow speed domain wall movement because of an apparent local annealing phenomena [20].

For materials such as 80 per cent Ni–20 per cent Fe permalloy, the uniaxial anisotropy is low enough so that rotational processes are feasible at reasonable fields.

With little transverse field applied ($H_T \ll H_K$) and with the switching field slightly larger than the coercive force, switching takes place by wall motion. This is a relatively slow process, as indicated in Fig. 2.

If a combination of transverse and longitudinal fields are applied so that the threshold for rotation is exceeded, reversal by nonhomogeneous rotation begins [16]. The threshold for nonhomogeneous rotation is usually operationally defined in terms of an abrupt change in the slope of the $1/T$ (switching time) vs H_L curve [3–5]. This break correlates very well with the value predicted from a simple single domain rotational model in which the anisotropy energy is characterized by a $\sin^2\phi$ function and the anisotropy is operationally determined by a susceptibility measurement in the transverse direction. In the nonhomogeneous switching region, part of the magnetization apparently switches by uniform rotation; the remainder of the magnetization switches by a slower process [9, 29]. If the uniaxial anisotropy field is given by H_K, the onset of rotation as

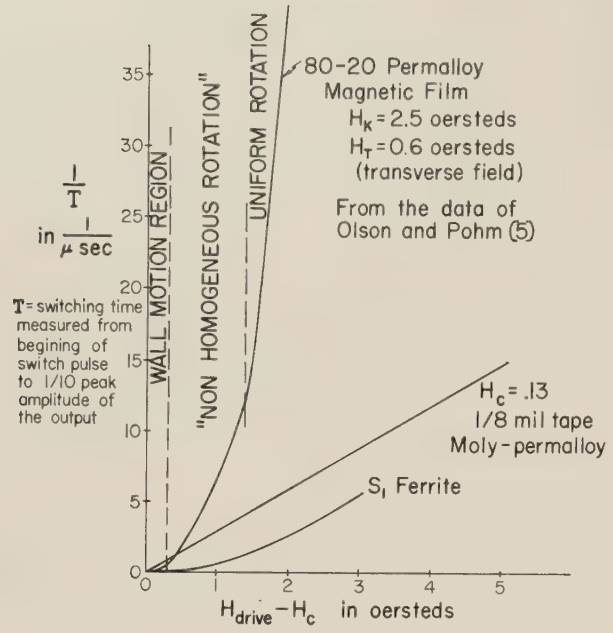


Fig. 2—Comparative switching characteristics of various materials.

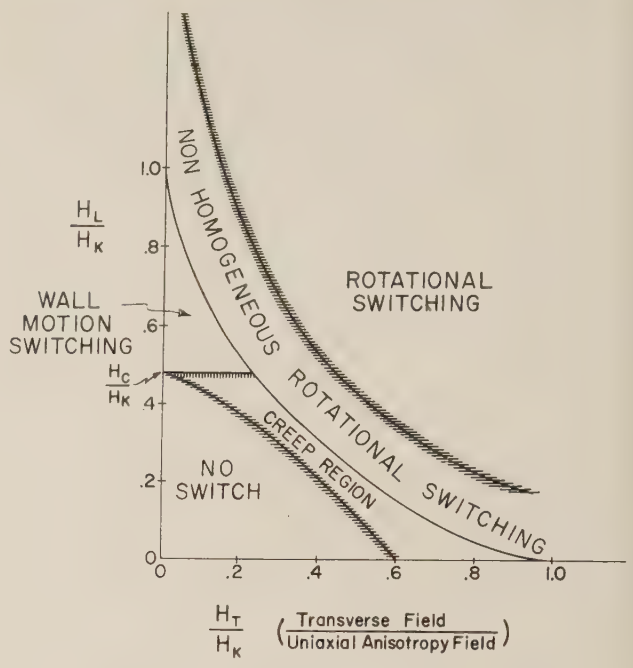


Fig. 3—Film threshold properties.

function of H_L and H_T is given for the simple model by the following parametric equations:

$$\frac{H_T}{H_K} = \sin^3 \phi, \qquad \frac{H_L}{H_K} = \cos^3 \phi.$$

Because of the imperfections of the material, the simple model is inadequate. The nonhomogeneous rotational switching process, although considerably faster than the wall motion process and the switching processes in ferrite and tape cores for normal drive fields as indicated in Fig. 2, is not as fast as predicted by the simple rotational model. Measurement of flux changes in the longitudinal and transverse directions show that most of the remagnetization is occurring by a rotational process, but not completely so [5, 16].

For longitudinal and transverse fields considerably in excess of the threshold value, and for rapidly rising fields, a second break occurs in the switching curve in which switching speeds approach that predicted by the simple model [5, 16, 29]. This simple rotation region is indicated in Fig. 2. With fields of a few oersteds, switching times of a few millimicroseconds have been observed, and switch slopes ($1/T$ vs H_L) in excess of 200 have been obtained [4, 5, 29]. Depending upon the operating conditions, this mode is 10 to 100 times faster than the mode normally characterizing ferrite or tape core switching as indicated in Fig. 2. Consequently, for very high speed memory operation, it is desirable to operate in the simple rotation mode.

The threshold characteristic for a typical permalloy film exhibiting the three main modes of switching is shown in Fig. 3 for various combinations of transverse and rest direction switching fields applied in the plane of the film [5]. Notice that if the nonuniform rotation threshold is taken as a reference, the wall motion threshold, the creep threshold and the simple rotation threshold may vary considerably with respect to it, depending upon the material and peculiarities of the sample and also on the test conditions. The uniform rotation threshold, for example, is sensitive to the rise time of the switching pulses and may vary considerably from sample to sample. The creep threshold (switching field values which will cause irreversible changes in the magnetization after repeated application) also varies from sample to sample and may depend upon the rise and fall times of the fields [11].

In the past, the nonuniformity of characteristics was evident not only from batch to batch but also from one film sample to an adjacent one in a single batch [18, 19].

III. Modes of Memory Operation

Beyond merely achieving higher speeds, thin magnetic layer storage elements possess three attributes (for both flat sheets and thin cylinders) which significantly enlarge their potential memory used beyond that available in a strung toroid memory. First, magnetically effective fields may be applied simply in either of the perpendicular directions [3] because of the small demagnetizing factors in the plane of the film; second, the thin geometry lends itself to etched wiring strip line techniques [5]; and third, a single storage element may be composed of two or more layers of magnetic material to achieve unusual and desirable memory properties [13].

1) The selection fields for switching can be applied in different directions with respect to the rest direction of the material giving rise to different performance characteristics and material requirements for satisfactory memory operation. As indicated in Fig. 4, if one of the memory selection fields is applied parallel to the rest direction (H_z) and one is applied perpendicular to the

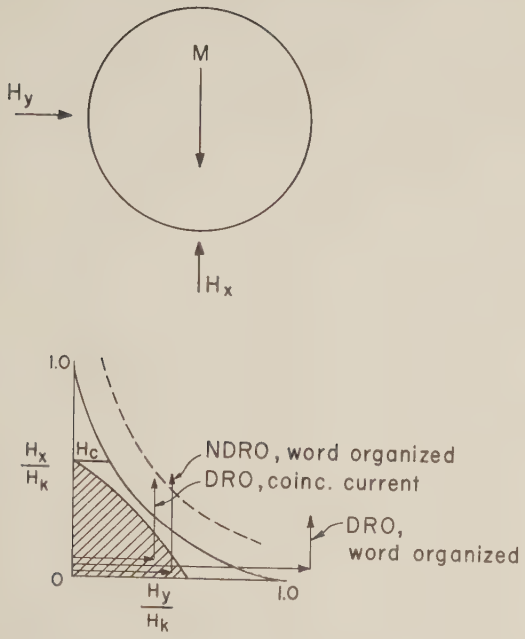


Fig. 4—Memory operation employing perpendicular fields. (NDRO = non-destructive read-out; DRO = destructive read-out.)

rest direction (H_y) a number of different modes of memory operation are possible. With this field arrangement and coincident current selection moderately high speed (in the fractional microsecond range), relatively small destructive-readout memories requiring good material uniformity can be made. The magnitude of the transverse field (H_y) is limited by the creep threshold and the unwanted signal from the half-selected cores. The longitudinal field is limited by the wall motion coercivity as indicated in Fig. 4. Since the transverse field generates an unwanted signal from the reversible rotation of the magnetization of the half selected cores, it is desirable to keep the transverse field as small as feasible. However, this imposes the restriction of a relatively high ratio of H_c/H_K. The optimum choice of the relative strength of H_x and H_y will be determined by the shape of the creep threshold, the simple rotation threshold and the attainable values of the H_c/H_K. As is the case with existing memories, the necessity of turning on an inhibit winding quickly after having read information imposes strong requirements on the electronics. In comparison to other memory modes, the material and electronic requirements are high for high-speed operation. One can expect therefore that only moderately sized high-speed memories of this type will be built. However, for slower speed operation where the unwanted signal from the half select transverse field can be allowed to decay before the longitudinal field is applied, one would expect that large coincident current memories can be built.

If this field arrangement is employed with a word-organized transverse field (H_y), the material requirements are lower and the material is normally capable of extremely high-speed operation since the transverse field can be made very large [7, 17]. The size and speed of this type of memory are determined primarily by the electronics. The delays in the sense and inhibit winding, along with the necessity of turning on the inhibit driver to rewrite information, limit the speed of operation. The full-select to half-select currents from the word select gates also impose a limit on size. Small memories with cycle time of 0.1 μsec or less appear feasible with this type of operation [7]. Larger memories (1024 words or more) in the fractional microsecond range appear also feasible for this type of operation.

This field arrangement also can be employed for very high-speed nondestructive readout memories in which a word select transverse field is used to give a nondestructive output [18], as indicated in Fig. 4. The longitudinal field is provided on a digit plane basis to accomplish writing. Since the reading is nondestructive, it is not necessary to have an inhibit winding which can be turned on rapidly. For writing, the two-polarity longitudinal field may have essentially the whole memory cycle to turn on and off. This type of memory operation consequently minimizes the electronic requirements as far as digit plane driving is concerned. Since the nondestructive output is considerably smaller than destructive output, more care must be taken to cancel unwanted signals.

For high-speed operation, the material requirements are high since the transverse field must be smaller than the creep threshold, and the longitudinal field must be less than the coercive force, while the combination of both should produce simple rotational switching. With optimum material modest sized memories with cycle times less than 0.1 μsec appear feasible. If the speed of a memory is limited by the electronic requirements or line delays, this is the fastest mode of operation. As this type of memory is made larger, the requirements on the selection gates becomes more stringent, and unwanted signal cancellation becomes more difficult.

2) If both selection fields (H_x and H_y), as indicated in Fig. 5, are applied parallel to the easy direction, magnetization reversal takes place primarily by the slower speed domain wall movement. The hysteresis loops for this mode of operation are extremely square [1, 2] and consequently are suitable for large memories. Since only the coercive force, thickness, and switching time are of primary importance for this mode of operation, the material requirements are less severe than in the rotational switching cases where the anisotropy field and creep threshold have to be controlled in addition. Large average-speed destructive readout memories with coincident current selection can be built requiring fair material uniformity with this mode of operation. If word selection is employed the material requirements can be reduced. Higher speeds can be achieved with this arrangement but at the expense of higher drive fields.

3) Memory operation can also be achieved by having selection fields parallel but at an angle to the rest direction of the magnetization as indicated in Fig. 6. In this way each selection field provides part of both the longitudinal and transverse field. Thus, for coincident cur-

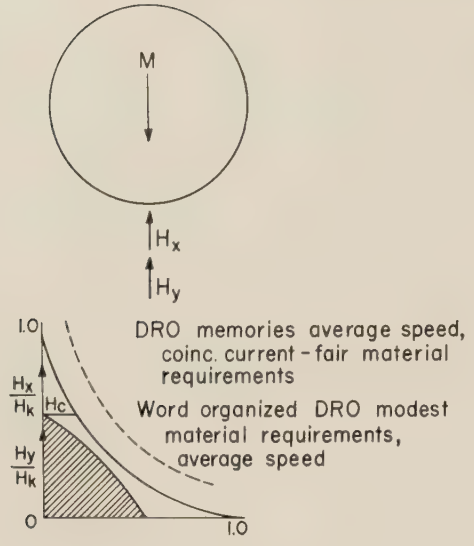


Fig. 5—Memory operation employing selection fields antiparallel to rest direction.

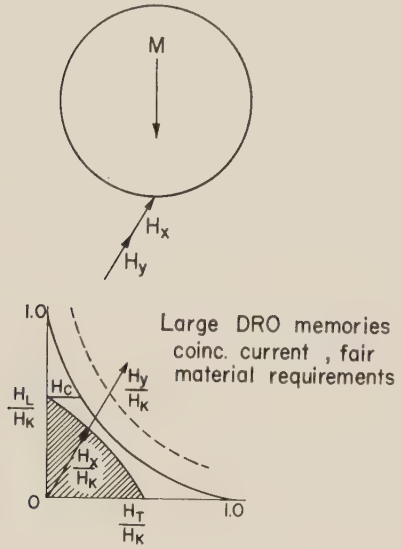


Fig. 6—Memory operation with parallel selection fields at an angle to rest direction.

rent operation, an angle may be chosen which will give optimum performance depending upon the magnetic material characteristics. In the case of half-selected elements, the angle of rotation is less than when one selection field is completely transverse. Since the pickup axis of the sense winding can be arbitrarily rotated, it is possible to choose a direction so that the change of flux linkages from a storage element about the sense winding due to a half pulse will be the same for a stored "one" and stored "zero." By alternating pickup polarity from element to element, good "delta noise" cancellation can be achieved [18].

With this type of field arrangement, large high-speed coincident current destructive readout memories can be made but require good magnetic material uniformity. This field arrangement could also be employed with a word selection system in order to reduce material requirements.

4) As pointed out, one of the attractive features of magnetic film memories is that the flat geometry lends itself to etched wiring circuit techniques. The top illustration of Fig. 7 illustrates how the necessary etched windings may be placed around the thin film storage elements to form low inductance two-wire strip lines. Since the relative positions of the memory elements can be fixed to very close tolerances, a winding for a whole memory plane can be formed at one etching. By laminating several layers, all the necessary windings are obtained for memory operation. By depositing the elements on thin susbstrates, the characteristic impedance and inductance of the two-wire strip line can be kept low [18].

The bottom illustration of Fig. 7 shows how two films may be combined to form a storage element with small air gaps [18]. By placing copper backing plates on the top and bottom, the drive lines essentially form three-wire strip lines which confine the electrical energy in a small volume. This type of arrangement is particularly suited for high-speed operation [18]. The double film core reduces the demagnetizing factor so that smaller core sizes can be used and the three-wire strip line prevents radiation of unwanted signals [18].

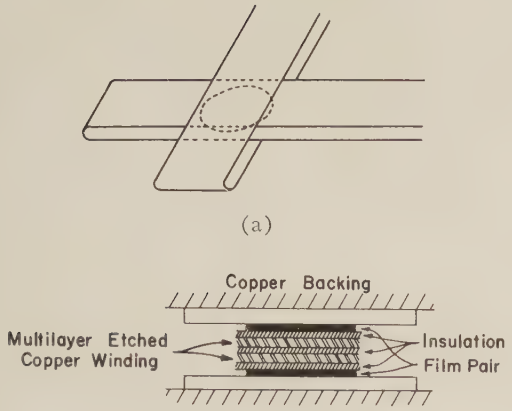
5) Fig. 8 illustrates how a pair of magnetic films can be combined to form a single nondestructive storage element as pointed out by Oakland and Rossing [13]. Normally the demagnetizing field from the divergence of the magnetization at the edges of a film gives rise to undesirable shear effects in the hysteresis loop. However, the demagnetizing field can be used to achieve desirable memory properties. In this particular example, a relatively thick, high-coercivity sample called the data film is chosen so that it has a relatively large demagnetizing field. The film thickness and size is chosen so that the demagnetizing field is large enough to switch the sensing film in a relatively short time so that its magnetization is antiparallel to that of the data film.

An interrogation pulse of insufficient amplitude to switch or disturb the data film but large enough to overcome the demagnetizing field and switch the sensing film is applied to achieve nondestructive sensing. If the data core is in the "one" state, the interrogation pulse switches the sensing film, and the demagnetizing field switches the core back after the interrogation pulse ceases. However, if the data film is in the zero state the interrogating field merely adds to the demagnetizing field and no switching takes place.

Notice [13] that the data film may be positioned to apply fields in different directions on the sensing film. The interrogating field may also be applied in different directions depending upon the particular mode of operation. This general effect of the demagnetizing field may be used for other devices.

IV. Material Problems

The magnetic films used for memories are typically made by vacuum deposition from a molten source on to



ig. 7—Etched wiring arrangement for magnetic film memories. (a) Films sandwiched between multilayer etched windings [5]. (b) Film pair 3-wire strip line arrangement [18].

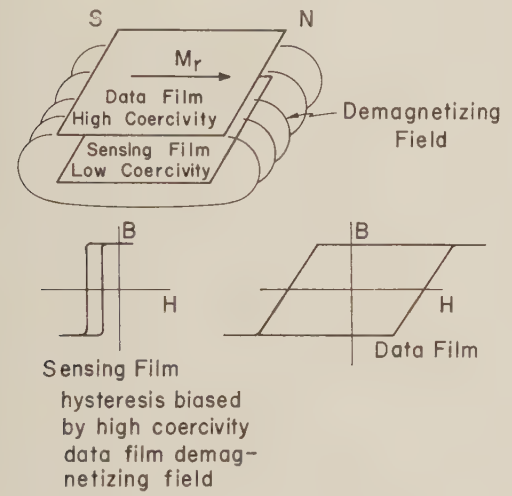


Fig. 8—An example of the use of film pairs with different properties to produce NDRO.

heated glass substrate in the presence of a magnetic ield or by electrodeposition of the alloy on to a conduc- ive surface in the presence of a magnetic field [1, 12]. n the former system one may heat the melt by induc- ion, resistance heating, or electron bombardment. At resent, the most common technique is to heat a slug of he proper alloy contained in a crucible by induction [18] or by evaporation from a tungsten filament. Both lc and ac orienting fields have been used successfully vith field values varying from 30 oersteds up to several undred oersteds.

The problem of control is a twofold one; for with any given parameter, a method must be found to achieve a specified value and then that value must be maintained within specified limits from sample to sample and batch to batch. One might argue that this last problem can be overcome by selection, but this sacrifices one of the attractive potential attributes of some film memories, namely, relatively easy and cheap production. A general list of the parameters to be controlled would include the coercive force (H_c), the anisotropy field (H_K), the total flux (ϕ), the rotational switching limit (creep threshold) and the switching time. The degree to which these parameters must be controlled and the difficulty of attaining the specified value depends on the particular application to which the film elements are to be put. To illustrate this we shall consider the general material requirements on the types of memories which have been discussed earlier in this article.

The requirement on total flux is such that one would like to have the films as thick as they can possibly be in order to improve the signal to noise ratio at the source without causing excessive shear in the hysteresis loops because of demagnetizing effects. At present the coercive force (which is a function of the thickness [19]), and the bit size (depending upon the arrangement) limit the thickness which can be feasibly used. The problem of uniformity in flux from spot to spot is largely a problem of making the individual spots of uniform thickness and, though this is difficult for large arrays, several alternative methods exist for achieving this [18].

As previously indicated, one high-speed memory mode employs reversible rotation of the magnetization. In this mode, the axis of magnetization is temporarily rotated out of the easy direction and then allowed to return, or the film is caused to switch by rotation. In the former case the creep region (see Fig. 3) should be minimized, for if the film is driven out into this region it will break down and not return to its original state. In permalloy this creep threshold tends to be low. Individual films have been made which rotate reversibly out to 60° but this type of film seems to be the exception rather than the rule [11]. In the case of true rotational switching it is necessary to reduce the size of the nonhomogeneous rotational switching region (see Fig. 3). While success in this matter with permalloy has not been outstanding to date, individual films have been made such that uniform rotational switching of a few millimicroseconds has been assured by the use of drive fields which were not more than twice the field required to produce wall switching [9] or creep.

In all memories discussed except those employing wall motion switching, the value of H_K must be specified and controlled to varying degrees of exactness. In permalloy films this value is typically of the order of three oersteds [9]. It does vary considerably about this value, and this variation is not completely understood. Generally, one wants to keep the value of H_K between 1.5 and 4.0 oersteds and the amount of variation about the median value that can be tolerated depends on the particular application. In the cases of the NDRO word organized memory (Fig. 4), the DRO coincident current memory (Fig. 4) and the memory of Fig. 6 the variation in H_K that can be tolerated is small. In the case of the DRO word organized memory the requirement is quite weak; the only requirement being that it not be too high. As a consequence this last memory is relatively easy to realize.

The control of H_c in permalloy is better understood than that of H_K. It is known that on a given film H_c

varies inversely with thickness [19]. H_c also depends on other factors, such as substrate cleaning procedures, etc. [19].

Some films appear to be temperature sensitive to the extent that their magnetic properties can be altered by the application of an appropriate orienting field while the film is maintained at an elevated temperature [10]. In the case of permalloy the films generally seem to be stable at temperatures below 75°C. At slightly higher temperatures the application of an orienting field perpendicular to the rest direction and in the plane of the film reduces the value of the anisotropy field. At sufficiently high temperatures (of the order of 200°C) the anisotropy of permalloy is completely destroyed and the hysteresis loop becomes square in both directions.

Because these films are generally made of a material which does exhibit magnetostriction [24], various magnetoelastic effects are observed as a consequence [18, 25]. If the magnetostriction is not zero, the magnetic properties of the films are sensitive to strain imposed externally to the substrate and consequently care must be taken to avoid introducing such strains in the fabrication of memories.

V. Outlook

At present, the biggest difficulty in producing a cheap satisfactory memory lies primarily with the materials problems. Of the types of memory operation discussed, those requiring minimum material uniformity have been developed to the greatest extent [7].

Since considerable effort is being directed towards understanding the basic reasons for the observed variation of characteristics with some success, one can reasonably expect that it is only a matter of time until these problems are resolved.

On the basis of material already made, and assuming the uniformity problems are solved, one can look forward to high-speed film memories with cycle times of less than 0.1 μsec at reasonable costs. One might also expect fractional microsecond or one or two microsecond cycle time film memories with many more than 1024 words. Published [18] techniques indicate that etched wiring can be made with "adequate" cancellation of unwanted pickup so that acceptable signals can be obtained. Recovery from digit plane transients can contribute significantly to the total cycle time.

VI. Acknowledgment

The authors wish to express thanks to their scientific colleagues for providing much of the information discussed.

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Some Applications of Magnetic Film Parametrons as Logical Devices*

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Summary—High-frequency magnetic film parametrons have en made and observed to exhibit two- or three-state operation for single bias condition. As a two-stable-state device, the magnetic n parametron can be used as a majority decision element in much same way as the ferrite core parametron. Another useful logical o-state device is a threshold element, in which the input excitation ust reach a minimum level to sustain oscillations. The magnetic n inductor, when suitably clocked, can be used as a gate to mit unilateral flow of information in a system. The gating action, ntrolled by the bias field, can result from the rectified output of a rametron. Proposed logical designs for a two-element binary adder, inary shift counter, and a shift register are presented. The possiities of three-state operation are also explored in the logical design a seven-element ternary full adder.

Introduction

N 1954, von Neumann [1] and Goto [2] independently proposed the use of phase-locked, subharmonic, parametric oscillators as logical elements computers. Since then, the work of Goto and others]–[7] has resulted in digital systems utilizing ferrite re parametrons. The low pump frequencies used mit these systems to relatively low speed operation. ecently the nonlinear capacitance of semi-conductor odes at microwave frequencies has been used to make phaselocked, subharmonic, parametric oscillator hich will operate at very high frequencies, permitting gital computations at near kilomegacycle rates [8]–0].

The authors have shown that a magnetic film parametron can be constructed using a time variable inductor made from 6×10^{-5} cm thick 80–20 permalloy ms [11]. The thin films used had a uniaxial magnetic isotropy axis perpendicular to their thin direction but all in magnitude. The films used were of suitable size, ickness and material, so that the magnetization in the agnetic material essentially formed a single domain in e remanent state with the saturation magnetic moent per unit volume M (gauss) lying in the plane of e film [12].

Fig. 1(a) illustrates such a single magnetic domain th external field h_s applied in the plane of the film rpendicular to the rest direction (the rest direction $\Theta=0$) and an external field H_p applied in the plane the film in the rest direction. The pump field, H_p, is nsidered to have a constant component, h_0, plus a

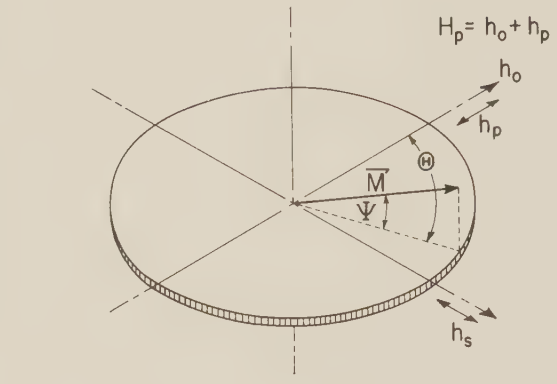

Fig. 1—(a) Thin magnetic domain with applied fields. (b) Magnetic film inductor.

time varying component, h_p ($h_p<h_0$). The angle Θ measures the rotation of the magnetization M away from the rest position in the plane of the film, and angle ψ measures the angle of rotation of the magnetization out of the plane. For usual materials and fields the large demagnetizing factor limits ψ to very small values. An inductor can be made by winding such a magnetic film deposited on a thin substrate with a pump and signal winding, as shown in Fig. 1(b). This inductor displays a time variable nonlinear characteristic which, when connected as part of a shunt-loaded tank circuit, makes operation as a phase-locked, subharmonic, parametric oscillator possible. If the parametron is tuned to one half of the pump frequency, the circuit will oscillate in either of two stable phase states 180° apart, for a particular pump field polarity and bias field (h_0) polarity. Another set, displaced 90° at the frequency of oscillation, is obtained if either the polarity of the bias field is reversed or the pump field inverted. The four possible stable phase states are shown in Fig. 2(a).

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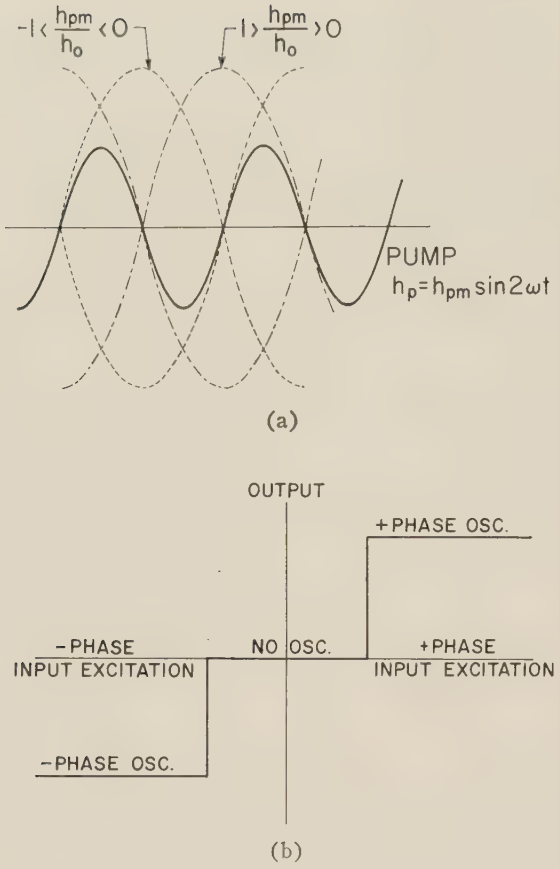


Fig. 2—(a) Four parametron phase sta'es. (b) Input-output characteristics of magnetic film threshold device.

It has also been shown [11] that the magnetic film parametron exhibits a hysteresis characteristic, which is a function of the frequency of oscillation and the magnitude of the pump field when the frequency of oscillation, ω, is greater than the resonant frequency of the tank circuit, ω_0. This hysteresis with respect to the pump drive also implies that for ω/ω_0 greater than the starting threshold for a specific pump magnitude, a certain input excitation is required for the oscillations to build up in parametron operation. For input excitation less than this, the oscillations will damp out. Fig. 2(b) illustrates these three possible states of plus phase oscillation, minus phase oscillation, and no oscillation as a function of input signal excitation.

The authors have shown that operation of the magnetic film parametron in the 100- to 500-mc region is feasible and a way of fabricating the parametrons with strip-line techniques is shown [13]. Using the etched strip-line circuit, one can use capacitive coupling between elements rather than conductive coupling with its attendant mechanical difficulties. Reversal of the bias on a film gives rise to subharmonic states shifted 90° from those obtained without the bias reversal and as a consequence, the near 90° phase shift introduced by the small capacitive coupling is just right to permit coupling into a second parametron which is reverse biased. The capacitive coupling technique also permits the simple extraction of either the function or it complement from the device.

Logical Device Operation

The bistable magnetic film parametron can be use for majority logic in essentially the same ways as th ferrite core parametrons employed by Goto and other [4]. Fig. 3 illustrates proposed configurations for th basic logical operations performed in parametron cir cuits. Of particular interest is the flexibility which basic circuit configuration gives the logical designer Rather complex logical changes in the operation o these circuits can be obtained simply by changing th "constant" parametron input. In Fig. 3(a) and 3(b either the AND function or the OR function is obtained depending upon the value of the "constant" input Likewise, the "exclusive or" function or its complemen describes the operation of the circuits in Fig. 3(c) an 3(d), respectively, the functional decision input agai being the "constant" input. The complemented input in the latter configurations both have a weight of 2 Complex logical changes in a system appear to b possible by specifying decision criteria for modificatio of the state of certain "constant" parametrons.

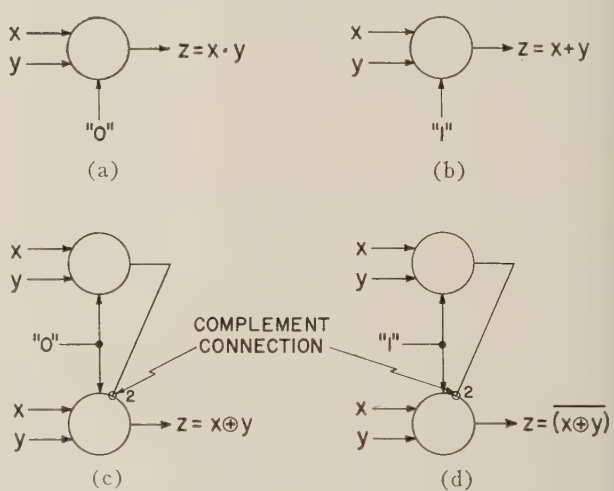


Fig. 3—(a) Basic AND configuration. (b) Basic OR configuratio (c) Basic EXCLUSIVE OR configuration. (d) Complement EXCLUSIVE OR configuration.

If the logical device is made using strip-line fabrica tion techniques, then information transfer betwee elements can be most efficiently handled by means the previously cited capacitive coupling method. Th would imply, therefore, that the bias would be reverse on alternate parametrons regardless of the clock pha to which the parametron is synchronized. In the logic circuits utilizing ferrite core parametrons, the flow information was synchronized with clock phase puls which gated the pump signal on and off. It would appe that this same effect can be obtained with magnet film parametrons by gating the bias field on and rather than the pump signal. The changing of the bi

eld would have the effect of detuning the tank circuit o stop the oscillations.

Another proposed use of the magnetic film paramtrons appears to be as a threshold element. As shown n Fig. 2(b), for a given pump drive and tank frequency, minimum level input signal is required for oscillations o be sustained. Therefore, for a given pump amplitude is possible to adjust the threshold of a parametron y controlling the bias field. The control of the bias eld makes two or three input threshold elements ealizable. Fig. 4 shows a threshold element and the otation to be used in the rest of this paper for the evice. A Roman numeral in the circle indicates the efective number of inputs of the same phase necessary o sustain oscillations. A number beside an input indicates the weighting factor of that particular input. A eighting factor of one is implied unless explicitly tated. In order to discuss the operation of this device, ssume that "1" represents one stable phase state, and 0" the other, 180° from the first. Therefore, this device an sustain oscillations in the "0" phase only if either or both) of the inputs, X or Y, are "0's." If both inuts are "1's," then the parametron will not oscillate. here is no way that this particular configuration can xist in the "1's" state.

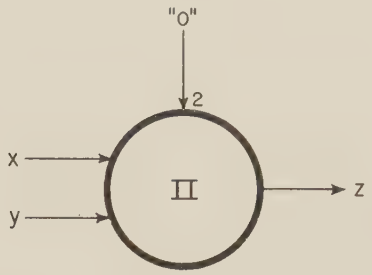


Fig. 4—Two-input threshold element.

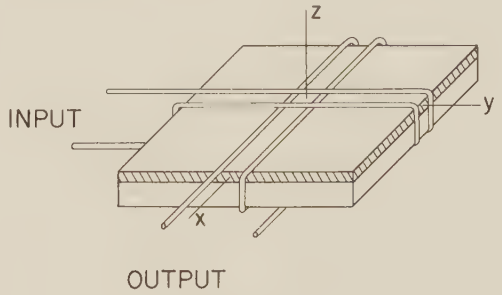


Fig. 5—Parametron gate.

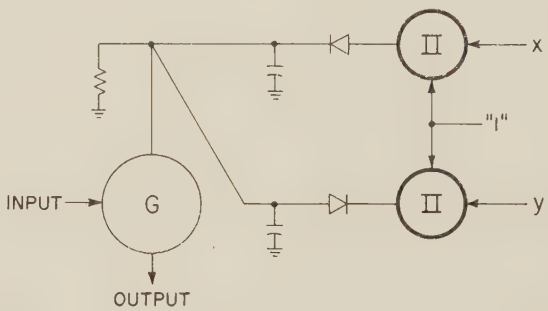


Fig. 6—Method for controlled gating of input with complementation.

Unidirectional Gating Element

The magnetic film inductor in a balanced modulator node [14] can be used as a unidirectional coupling lement or gate. An input winding is placed on the nductor so that the resultant field from an input signal ies in the easy or rest direction of the magnetization ector. The output winding is placed perpendicular to he input winding so that its field is in the hard or ransverse direction. The physical arrangement is shown n Fig. 5.

If only the input signal is present there can be no oupling to the output winding and, hence, no gate or ransfer action. However, if a bias current is introduced nto the output winding or into a winding physically arallel to the output winding, the magnetization vecor will be rotated out of the rest position. The field of he output winding is in phase or out of phase with the nput, depending upon the direction of the bias current. n this manner it is possible to couple out the gated ignal or its complement. Because of the configuration f the inductor and bias timing, the gating action is nilateral. The use of such gating elements would eliminate the need for the third clock phase in the circuits described by Goto using ferrite core parametrons.

Several possibilities using other parametrons as threshold elements to control this gating function are proposed in Fig. 6. The outputs of the threshold elements are rectified by the diode capacitor combinations to supply the bias for the gating element. In this method the output would have the same phase as the input when X is "1" and Y is "0," and the opposite phase as the input when X is "0" and Y is "1," the bias being reversed in these two input combinations. No output is available when both X and Y are "0's" or "1's." Permuting the states of the threshold elements, the polarity of the diodes and the state of the gate inductor film permit many modes of operation within the same configuration. Controlled gating of this type can be very useful in the logical formulation of complete systems.

Logical Function Operation

A very simple binary adder using magnetic film parametrons is proposed. This adder is shown in Fig. 7. Both parametrons 1 and 2 are simple majority decision elements. The input to 1 are the addend X_i, augend Y_i, and the carry from the previous state C_{i-1}. The output of 1 is the carry to next stage. The additional input to 2 is twice the complement of C_i. The output of 2 is the sum. Depending upon the speed of the two parametrons, it may be necessary to clock 1 before 2 to insure that the majority decision is made in 1 before 2 breaks into sustained oscillation. This same result can be obtained by using the output of 1 to gate the inputs of 2.

A relatively simple shift counter is also proposed using magnetic film parametrons. A proposal for the first three stages is shown in Fig. 8(b). Fig. 8(a) shows an intermediate stage of such a counter. It is seen to be a simple full binary adder, such as the one described before, with a fixed zero as one of the inputs. The shift counter is little more than a logical adder in which the present sum is formed between the previous sum and a fixed addend. The first stage of the counter needs simply to be a complementing circuit gated by the shift signal itself. In Fig. 8(b), parametrons 1, 2, and 3 are used as

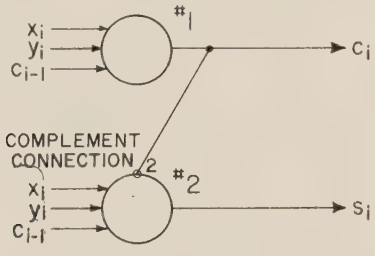
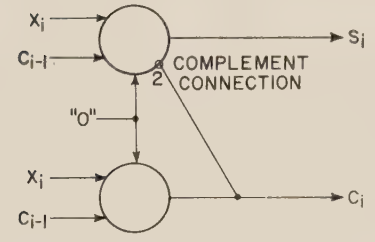
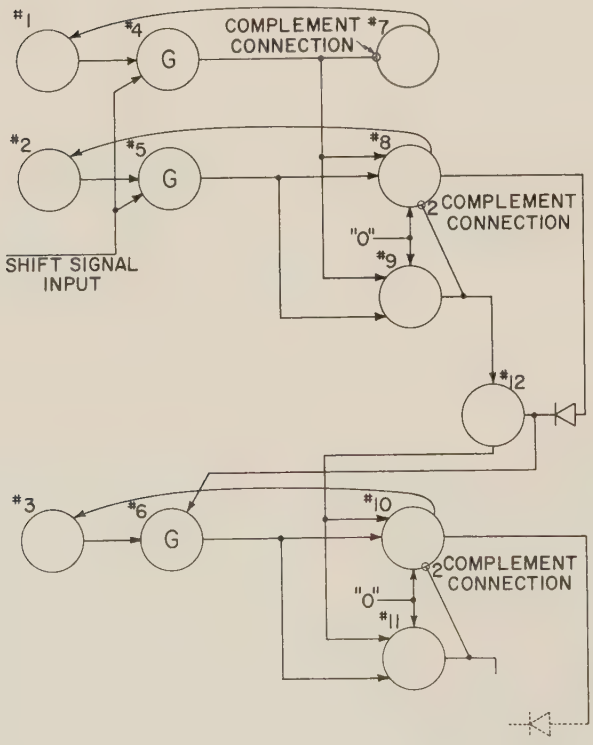


Fig. 7—Binary full adder.



(a)



(b)

Fig. 8—(a) Intermediate stage of a shift counter using magnetic film parametrons. (b) First three stages of a shift counter.

temporary storage elements, and their contents are considered to represent the number of shifts performed. A rectified shift signal can be used to gate the contents of parametron 1 plus one and parametron 2 to parametrons 7 and 8 without problems of delay. The rectified oscillations of 8 would then be used to gate the contents of 3 through 6, and the output of 9 through 12. Likewise, the output of 10 would be used to realize the gating necessary in the next state. When suitable delays have occurred to permit parametrons 7, 8, 10, etc., to hold the new number, parametrons 1, 2, 3, etc., must be turned off. Then the new number can be gated into 1, 2, 3, etc., simply by restoring the bias field to its normal value.

A shifting matrix would be quite simple using only parametrons and gates. One proposal is shown in Fig. 9.

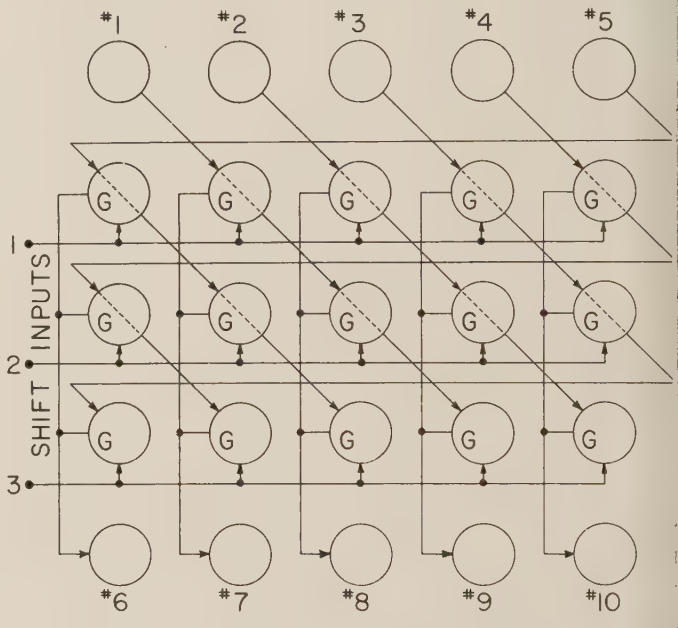


Fig. 9—Shift matrix.

The contents of 1, 2, 3, 4 and 5 can be shifted one, two or three places to the right, depending upon which one of the three dc bias windings labeled shift inputs are excited. The RF input windings on each of the gates are connected in series as shown. The separate output windings are also connected in series. A noise signal at twice the parametron frequency is generated in each of the unselected gates because of this configuration, but the level will be low and thus will not affect the state of the parametron. It is also possible in an auxiliary circuit to gate the contents of the parametrons in the bottom row straight up to the top parametrons after the shifting operation is finished, and the oscillations in the top parametrons are damped.

A Ternary Full Adder

One of the more interesting aspects of magnetic film parameters as logical elements is the possibility of being able to utilize the three state operation of the device

ig. 10 shows a proposed ternary full adder. The three ates of operation have been defined in the following ay:

"0"—no oscillation
"1"—oscillation in phase with reference
"2"—oscillations 180° out of phase with reference.

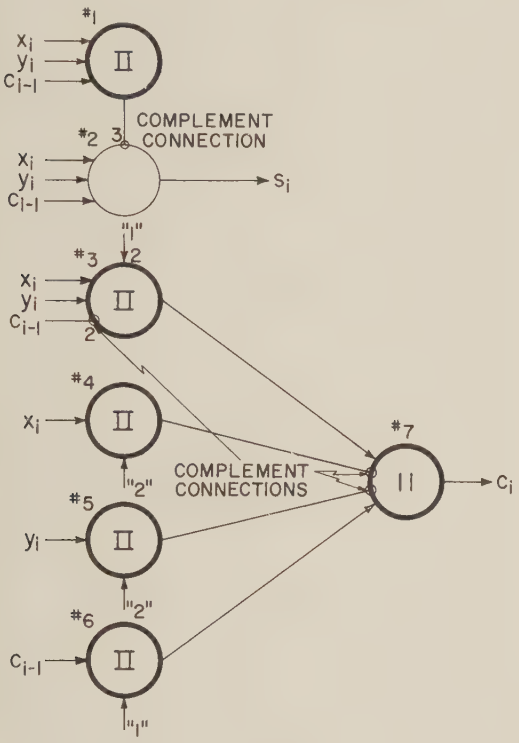


Fig. 10—Ternary full adder.

Also, for the three-state element, "complementation" is lefined simply as a phase inversion of the signal. Therefore, the "complement" of "0" is "0"; the "complement" of "1" is "2"; the "complement" of "2" is "1" under this definition. Two input threshold elements are used as six of the necessary seven parametrons. Parametron 2 is a majority decision element whose output is the new sum. The inputs to parametron 2 may need to be gated by the output of parametron 1 if a race condition exists at this point. It is possible that if the inputs to all of the parametrons are energized simultaneously, the mode of operation of 2 could be determined by inputs X_i, Y_i, and C_{i-1} only. Normally this mode of operation would be in error unless the output of 1 is "0." Therefore, it may be necessary to gate in all four inputs into 2, simultaneously. This could be done by using the rectified output of 1 to provide the bias for a gate. The adder, as shown, will produce the correct sum and carry to the next stage for any combination of the inputs that are realizable. Only 18 of the 27 possible combinations of inputs need be considered, because the carry into the stage can never be two.

The use of threshold elements in this adder is particularly useful because the addition can be performed in one clock phase. Of course, in any element in which one must rely upon the summation of wave forms in order to perform a logical operation, there will always be a problem of phase shift caused by path length, etc. However, for threshold elements one can reduce the problem of decision making before all of the inputs exist. Even so, attention would have to be paid to this effect if one were to build a 30-stage adder without provisions for carry propagation other than permitting the carry to ripple through the whole adder. Any parametron should reach steady state operation within ten cycles of the pump frequency, after conditions for sustained oscillations exist. In most cases, if some care is used in selecting the phase of the input, steady state can be reached much sooner. Certainly then, a clock pulse time of 50 cycles would be sufficient to form the sum and carry in each stage of such an adder. Additional time may be necessary for carry propagation depending upon the method used.

The truth table for the ternary full adder is shown in Table I.

TABLE I
TRUTH TABLE FOR TERNARY FULL ADDER

X_i	Y_i	C_{i-1}	S_i	C_i
0	0	0	0	0
0	1	0	1	0
0	2	0	2	0
1	0	0	1	0
1	1	0	2	0
1	2	0	0	1
2	0	0	2	0
2	1	0	0	1
2	2	0	1	1
0	0	1	1	0
0	1	1	2	0
0	2	1	0	1
1	0	1	2	0
1	1	1	0	1
1	2	1	1	1
2	0	1	0	1
2	1	1	1	1
2	2	1	2	1

Conclusions

Since a magnetic film parametron can be used in two- or three-state operation, it has great potential as a logical element in both binary and ternary systems. In two-state operation one very effective and useful way of employing this device is as a simple majority decision element. There are several problems directly connected with this particular method of utilization. First there is the relative phase relationship between the inputs. In the ideal case, each input would be in phase or 180° out of phase with some reference. The summation of the input waveforms would indeed be indicative of a majority decision in this case. However, because of path lengths, etc., this condition generally will not exist. The limits of relative phase shifts for

reliable operation have not been determined.

Another problem, inherent in a majority decision element, concerns the timing of the inputs. Once a parametron begins to oscillate, only removing the pump or detuning the device can squelch the oscillations. Therefore, the timing of inputs to such an element may be critical.

The threshold element essentially bypasses this second difficulty. It can not sustain oscillations until sufficient input is present. Timing is important here only as it affects the phase relationship of the inputs. It would appear that on some occasions one might change the threshold level of a given element by varying the bias field, depending upon the past history of the element or its environment.

The parametron gate appears to be a particularly useful device. It permits the unilateral flow of information, thus reducing the number of clock phases necessary in a system. It also permits one to regulate and direct the flow of information, depending upon what is occurring in other elements or parts of a system.

It would appear that parametron devices could be used to advantage in medium speed systems. Certainly the number of components required to perform operations such as binary addition is smaller than in present systems. Fabrication of devices to perform these logical functions using strip-line techniques should not be too difficult. The properties of a film used in this mode are not particularly critical. Certainly they are much less stringent than those for operation as part of a film memory.

This device is one of the few that can exist in more than two unique stable states, and in addition, there is power gain available in each element. It would appear that investigations of ternary logic may be more reasonable now that such devices do exist. The ternary full adder is an example of what can perhaps be done along this line. More effort in these areas is warranted.

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A Thin Magnetic Film Shift Register*

KENT D. BROADBENT†

Summary—An initial application of the dynamics and interactions of domains within continuous magnetic thin film structures is made to a shift register in which binary information is stored and translated in and along a continuous evaporated thin magnetic film. These thin magnetic film shift registers are capable of storing information having a density of several hundred bits per square inch of vacuum evaporated structure and of translating this amount of information at bit rates in excess of a megacycle with powers of less than 10 watts.

Introduction

THE dynamics and interactions of domains[1] within continuous magnetic thin film structures may be applied to a variety of information processing or computing functions. A useful initial application of this concept is to a shift register in which binary information is stored and translated in and along a continuous evaporated thin magnetic film. This operation may be pictured as analogous to a magnetic drum surface on which the "bits" move instead of the drum. The basic simplicity of continuous shifting systems which eliminate the usual cell to cell coupling networks makes such an approach extremely attractive. Magnetic shifting involving continuous wire structures has been reported.[2] In the film system to be described, the very-high-volume density of stored information, the low power of operation, the relatively high speed of operation, and the automated production potential indicate unusual system possibilities.

Theoretical Considerations

The operation of this device can be explained, in a preliminary way, on the basis of a difference which can be made to exist between the energy required to establish or create a particular domain configuration within the magnetic continuum, and the energy required to translate the given domain configuration a distance through the continuum. This difference allows "written" domains to be moved unilaterally under the influence of periodically pumped forcing fields without these fields introducing any spurious information.

The specified energy difference may be inferred from the following considerations. The creation energy for establishing a given domain configuration within a magnetic continuum contains conservative terms such as the magnetostatic, magetocrystalline, and exchange energies, as well as the dissipative terms associated with switching the magnetic material. The translation energy for moving a given domain contains only a dissipative energy term, with the conservative terms remaining constant (provided that the domain is translated within a uniform magnetic continuum under conditions which preserve its domain configuration and relation to its environment). Considering the control that can be exercised over these various components, a design may be selected in which it is possible to drive propagating electrodes hard enough to move domains, but not hard enough to create domains. The domain is created by a separate writing electrode and current.

A more complete consideration of the operational theory of this device must also take account of certain "rate factors," such as domain nucleation times and wall motion damping effects. These factors become increasingly important in the design of maximum speed registers.

Propagation of a domain through the magnetic film consists of translating the walls of the domain in phase to preserve the essential domain configuration. One combination of magnetic film and electrode structure for achieving this shifting action is represented in Fig. 1. Fig. 2 is an exploded view of this vacuum deposited configuration. This configuration provides means 1) for supplying the creation energy to the magnetic film through application of current to the writing electrode, 2) for supplying propagating energy to the magnetic film through application of current to the propagating electrodes, and 3) for detecting the flow of domains through the induced voltage in the readout electrode looping the magnetic film.

The configuration's operation in moving "written" domains under the influence of periodic, continuously pumped forcing fields is shown in a series of longitudinal cross sections of Fig. 3. Row 1 of Fig. 3 shows the shifting configuration with its magnetic film magnetized to the right throughout. Current is passed through the writing electrode with a direction and magnitude to reverse the magnetization of the magnetic material lying under its influence. This brings about the condition of the magnetic film shown in Row 2. Row 3 represents the translated state of the domain after current of the proper magnitude and sense has been passed through the upper propagating electrode set. The arrows indicate the alternating H field pattern set up by the flow of the current. These fields are seen to be of the proper polarity in the vicinity of the domain walls to induce

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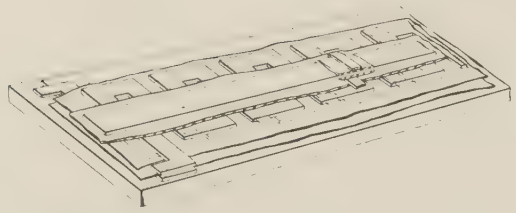

Fig. 1—Artist's sketch of the vacuum evaporated thin film shift register.

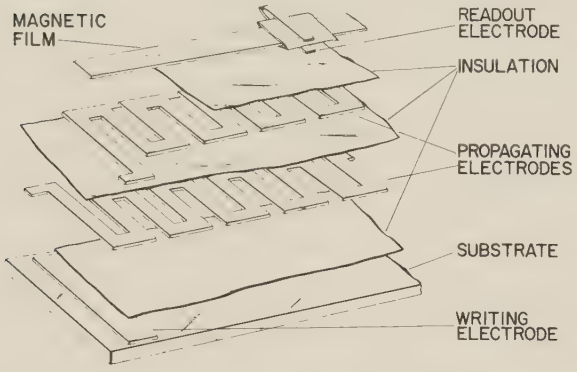

Fig. 2—Exploded view of the thin film shift register.

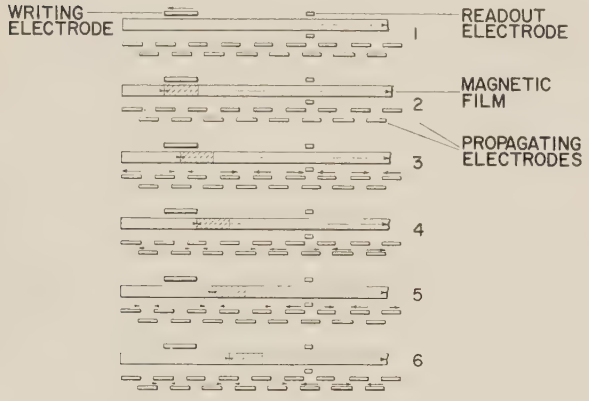

Fig. 3—A series of longitudinal cross sections demonstrating the propagating-current pattern and the shifting sequence of the register. The cross-hatched area represents a domain of reverse magnetization within the continuous magnetic film.

wall motion in the appropriate direction to translate and preserve the domain. This translation brings the domain into proper position with respect to the lower propagating electrode set. Row 4 represents the further translated state after the application of current to the lower electrode set. For the next translation, a reversed current is required through the upper propagating electrode bringing about the configuration of Row 5, and the next translation to Row 6 requires a reversed current in the lower propagating electrode. The domain is now in a position for the pattern to be repeated.

This basic four-beat propagating pattern provides the unilateral flow of domains and may be pumped continuously. Because of its subcritical field nature, the pattern is effective only in moving established domains and not in creating or establishing new domains. Obviously, the direction of information flow may be reversed by reversing the propagating pattern. Because of the spacing and width of the information domains within a single magnetic strip, four propagation pulses are required to transport the complete bit configuration past a particular fixed reading station. A register in which information may be read at every propagating pulse time is realized by using four magnetic strips in parallel with offset READ and WRITE electrodes.

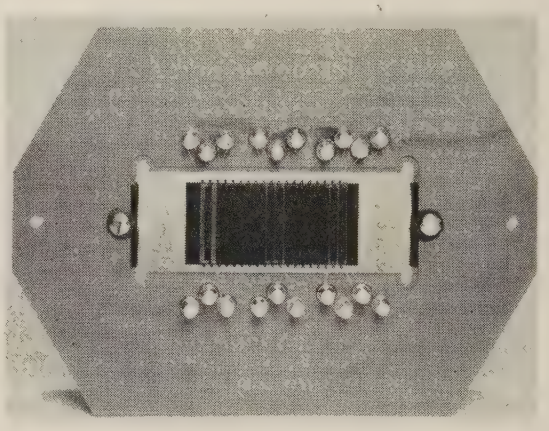

Fig. 4—A photograph of an experimental vacuum evaporated shift register. The register measures 1.5 inch×0.9 inch.

Experimental Registers

Fig. 4 shows an experimental thin film shift register which has been operated at propagating pulse frequencies in excess of one megacycle. This register was produced using sequential vacuum evaporation techniques[3] in depositing magnetic,[4] conducting, and insulating materials in patterns corresponding to Fig. 2. The magnetic material is deposited in an orienting magnetic field giving a preferred direction of magnetization along the length of the strip. The sequence of deposition shown in Fig. 2 was inverted, with the magnetic strips lying nearest to the substrate. The information is translated 0.020 inch during every propagating pulse, permitting 50 bits to be stored in one linear inch of the shift register. Several of these registers may easily be placed side by side in the space of one lateral inch and may be driven by a common set of propagating electrodes. In practice, this provides a surface storage density of several hundred bits per square inch.

The power required to drive a register is set primarily by the resistance of the propagating electrodes. The register of Fig. 4 requires a power of 8 watts for operation at a megacycle and 2 watts for 100-kc operation. The propagating electrode currents are 0.45 and 0.90 ampere respectively, giving H fields at the surface of the magnetic strip of 3.7 and 7.4 oersteds.

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Using a magnetic strip having a width of 0.040 inch, ur registers (comprised of four strips each) can be aced under the propagating structure visible in Fig. 4. he pictured unit has a capacity of 300 bits. The propa- ting electrodes are 0.030 inch wide and spaced 0.010 ch apart, the writing electrode is 0.040 inch wide, and e readout electrodes are 0.005 inch wide. The conduct- g and insulating layers range from one to three mi- ons in thickness. The magnetic strips are 900 A thick, mposed of 75 per cent nickel and 25 per cent iron, and he electrical output signals at a megacycle rate are out 1 mv in amplitude. Greater densities or larger out- uts may be achieved with other designs.

The configuration of the information bit in the mag- etic strip may be varied widely, depending upon the mbination of geometric and material factors em- loyed. Exceptionally high bit density registers may be perated in which the information bit is a single quasi- lliptical domain. Other registers show the bit to be a luster of elliptical domains and still others may be perated with a semirectangular domain having a fine- tructured domain boundary. Examples of these con- gurations are shown in Fig. 5. Photographs of the do- nains were obtained using the Kerr magneto-optic effect.[5] This device and its operational principles are covered by a United States Patent.[6]

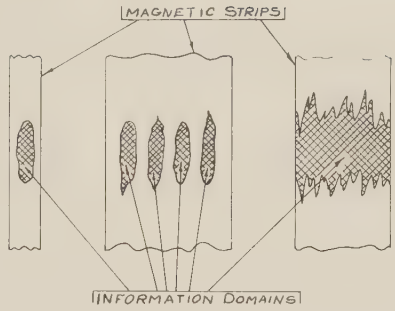

Fig. 5—Facsimiles of magneto-optic Kerr photographs showing domains within various evaporated shift register strips.

ACKNOWLEDGMENT

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Fluxlok—A Nondestructive, Random-Access Electrically Alterable, High-Speed Memory Technique Using Standard Ferrite Memory Cores*

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Summary—**The Fluxlok memory technique uses the principle of ross-field magnetization to achieve the nondestructive sensing of he information state of standard, readily available, ferrite memory ores in a simply wired memory plane. Bipolar output (ONE and ERO) signals are obtained at the rate of rise of the READ pulse. he signals are unaffected by test temperatures of from −65°C to +100°C. Coincident current WRITE operation or an inherent orthog- nal field WRITE may be used. A 2-mc 64-word Fluxlok memory est vehicle is described.**

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INTRODUCTION

THERE have been many nondestructive storage devices described in the literature using rotation of magnetic moments instead of domain wall motion to produce an output pulse when read. These methods have the general advantage of very fast READ rates, since the magnetic moments will rotate at essentially the rate of the READ pulse rise time. Past art, in many cases, has resulted in very small output signals, critical read pulse width and amplitude requirements, and/or unique and complicated device geometry.

The Fluxlok memory technique provides electrically alterable, random-access, high-speed, nondestructive

READ. Standard ferrite memory cores are used in a simply wired memory plane configuration. The technique employs the principle of orthogonal magnetic fields to provide READ rates exceeding 10 mc, with no apparent core heating effects. Read is accomplished by a single unipolar pulse of noncritical duration, amplitude, and polarity. Relatively large bipolar output signals are obtained at the rate of rise of the READ pulse. The output signals have been found to be insensitive to tests at temperatures from −65°C to +125°C, and operation within substantially wider extremes appears to be quite feasible.

READ rates of about 500 kc are obtained with the use of transistor drivers and X-Y selection switches, the upper limit being determined by the present state of the semiconductor art. Thus, the Fluxlok memory is not device-limited, but rather it is circuit-limited at the present time.

Information may be written into the memory in conventional coincident-current fashion, or by means of a slower but much simpler orthogonal write capability, inherent in Fluxlok. In the orthogonal WRITE operation, the same drivers may be used for READ or WRITE, since the operations are identical except for the absence or presence of information current in the sense lines. Information drivers can become a part of the computer memory ground loading equipment in airborne or spaceborne computer applications where stored information is not required to be electrically alterable during flight. The configuration of windings and application of currents are such that noise or power supply transients cannot effect changes in the memory content.

The simple wiring configuration employed permits firm mounting of memory cores, relatively rapid and inexpensive fabrication of memory planes, and reasonably high packing density. Only the sense winding need be threaded through the memory cores; other windings pass directly across the core faces.

The capability and reliability afforded by the technique have been demonstrated in a 2-mc, 64-word Fluxlok memory test vehicle developed under government contract. Modifications which give a substantial reduction in the READ pulse power requirement have been developed.

Fluxlok Nondestructive READ Principles

Perhaps the most important feature of the Fluxlok technique is the use of highly-standardized and readily available ferrite memory cores in a unique wiring matrix that provides the nondestructive READ capability.

The basic premise of Fluxlok operation is illustrated in Fig. 1. Two equal windings (L_1 and L_2) of a READ solenoid are wound on a toroidal magnetic core in series opposition. A sense line threads the core. If a current pulse of any arbitrary duration and amplitude is passed through the opposing windings, a magnetizing force is produced, but the corresponding circular mmf's in the core cancel one another during the period of the pulse (as indicated by the dotted arrows), and the remanent state of the core (existing prior to the application of current) remains the same when the current is removed. (There is little irreversible flux change.) For computer memory applications, the remanent state of the core is typically near one of the two zero mmf points on a steady-state hysteresis loop, corresponding to a ONE or ZERO in binary logic.

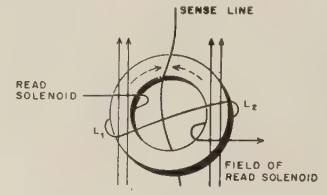

Fig. 1—Conceptual form of Fluxlok READ solenoid.

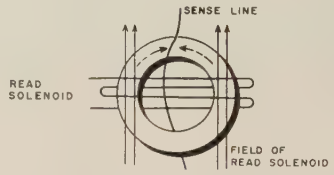

Fig. 2—Actual form of Fluxlok READ solenoid.

Fig. 2 shows another way of placing a *single* READ winding around the *outside* of a magnetic core so that the mmf from a pulse of current in the winding produces little irreversible change in the remanent state of the core. The field from the READ solenoid sweeps broadly across the core producing the same effect as in Fig. 1, and again there is no circular mmf applied to switch the core. However, in both cases, examination of the sense wire during the READ pulse reveals that during the rise time of the pulse, a strong output signal appears on the sense line with a polarity directly corresponding to, and solely dependent upon, the ONE or ZERO state of the core. An output signal equal in amplitude, but opposite in polarity, is produced during the fall time of the pulse.

Memory Organization and Fabrication

The wiring configuration of Fig. 2 is preferred to that of Fig. 1 in memory organization because of the very simple memory plane made possible by this method (Fig. 3). Ferrite cores are securely mounted (side by side, rather than face to face) into preformed holes in a phenolic memory plane, sense wires are threaded through the cores, and word solenoids are wound around the outside of the board transversely to the direction of the sense wires. The sense lines can be threaded through each core twice, in a transposed fashion as shown, to produce larger output signals and to provide common mode noise cancellation. The packing density, using 50/80-mil cores, is approximately 1000 bits per cubic inch.

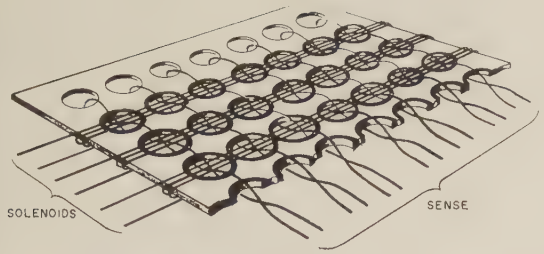

Fig. 3—Fluxlock memory plane configuration.

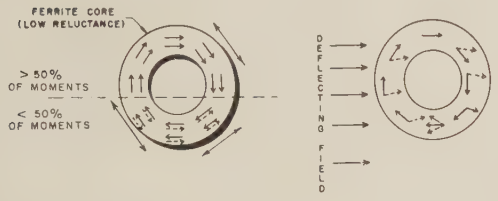

Fig. 4—Concept of magnetic moments.

Basic Theoretical Assumptions

Referring to Fig. 4, one theoretical explanation of the magnetic phenomena inherent to the Fluxlok technique requires that the following assumptions be made:

1) Tiny magnetic moments exist throughout any material; however, in most materials, neighboring moments cancel and a net balance of magnetic moments, or zero magnetism, is exhibited.
2) In some materials, such as ferrites, this cancellation is incomplete; the sum of moments in a small region tends to be aligned in a common direction, thus exhibiting a significant net magnetism.
3) In a toroidal ferrite core, moments have a preferred orientation in a direction tangent to the path of least reluctance. The flux prefers to remain within the core rather than traverse a high reluctance path through air.
4) If more than 50 per cent of the magnetic moments in the core are oriented tangentially to either of the circular flux paths of normal remanence within the core, their collective action tends to induce the remaining moments to assume the majority state.
5) These magnetic moments may be slightly rotated to a position differing from their preferred position by the application of an orthogonal magnetizing force. (The mechanism of the more conventional method of applying mmf—by linking the toroid—is quite different.)
6) Upon termination of this deflecting field, the moments realign rapidly to their initial preferred orientations.
7) If the majority of the moments have been rotated more than 90° by the deflecting field, realignment is in the opposite direction. However, it appears to be quite difficult to produce net moment rotations of greater than 90° with this method of applying mmf; demagnetization of the core appears to be the more likely ultimate result of severely increasing the orthogonal mmf.

Read Operation

Nondestructive READ is accomplished by passing a suitable current through a word solenoid which surrounds the row of cores to be read. With a core initially magnetized in the clockwise direction shown in Fig. 5(a), the application of the H field [Fig. 5(b)] produces rotation of the magnetic moments. The moments now complete their flux paths through air. Creation of air paths by the H field produces a net decrease in the flux within the core, and a voltage of fixed polarity is induced in the linking sense wire. When the H field is removed, the B vectors snap back to their original position, thereby inducing a second output voltage equal in amplitude but of the opposite polarity. With the core originally magnetized in the counterclockwise direction [Fig. 5(c)], the H field causes rotation in the direction [shown in Fig. 5(d)] and the polarities of the two output voltages are reversed.

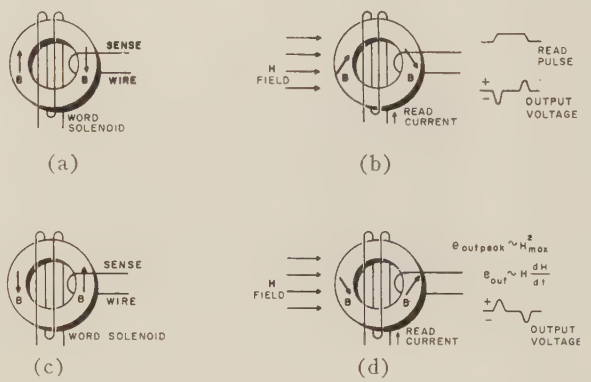

Fig. 5—Nondestructive READ operation. (a) Core at ZERO remanence (clockwise flux path). (b) Application of READ current. (c) Core at ONE remanence (counterclockwise flux path). (d) Application of READ current.

The *polarity* of the output voltage (rather than the amplitude, as in most core memories) indicates the *state* of the core. The output voltage (e_{out}) is directly proportional to the time derivative of the square of the solenoid field; that is,

$$e_{out} \sim H \frac{dH}{dt} . \tag{1}$$

This experimental fact can be justified by considering the expression for flux linking the sense winding,

$$\Phi = \int_A B \cos\theta dA, \tag{2}$$

where B is the flux density and θ is the angle between the vector B and the normal to the surface element dA. As Fig. 5 suggests, application of H tends to rotate an approximately constant B through some small angle θ.

To a first approximation then we expect that there will be a change in flux ($\Delta\Phi$) satisfying the following approximate proportionalities

$$\Delta\Phi \sim (1 - \cos\theta) \doteq \frac{\sin^2\theta}{2} \qquad (\theta \text{ small}) \tag{3}$$

and

$$H \sim \sin\theta. \tag{4}$$

From

$$e_{out} = d\Phi/dt, \tag{5}$$

we then get the approximate result

$$e_{out} \sim H\frac{dH}{dt}; \tag{6}$$

if the shape of the solenoid pulse stays constant so that dH/dt stays proportional to H, then

$$e_{out\ peak} \sim H_{max}^2. \tag{7}$$

Fig. 6 shows the waveforms taken from a memory plane being read at a 2-mc rate. Faster rise time interrogate pulses would, of course, produce higher-amplitude output signals.

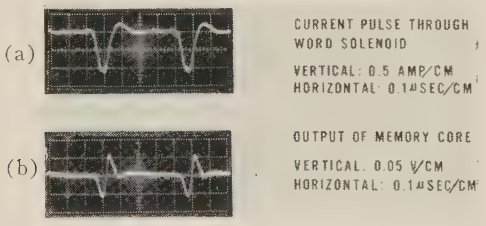

Fig. 6—Driver and memory core output waveforms.

Discussion

READ is nondestructive because the H field only partly rotates the B vectors of the cores. When H is removed, the high reluctance of the possible return paths through air constrains the B field to revert to the core and return to prior remanence. Experimentally, the H field may be several times greater than that used in normal memory interrogation before producing any noticeable demagnetization. Consequently, memory is not destroyed during READ. Cores have been read with this technique more than 10^8 times with no destruction of information. As noted in Buck's article,[1] a transient effect is produced, in that the first output voltage from a freshly magnetized core is about 20 per cent higher than those following in a chain of repetitive READ pulses. Although Buck's article describes the application of currents down the length of the wraps of magnetic tape wound cores, and the application of crossed fields to sectors of these cores by the use of separate gapped-core electromagnets, the basic principle involved is the same as in Fluxlok—orthogonal magnetic fields. Buck also gives credit to Jenney (M.I.T.) for the conception of drilling nonintersectiong orthogonal holes through ferrite cubes to provide a nondestructive memory element.

Gianola[2] is to be credited with the early nondestructive READ of a domain oriented steel sire. He presented a method of reading ferrite cores nondestructively that differs from Fluxlok mainly in the plane of application of the orthogonal READ field. He applied the READ solenoid winding around the circumference of the core, rather than diametrically across the face as in Fluxlok. He also described a form of orthogonal write.

Thorenson and Arsenault[3] conceived and published the idea of drilling two opposing holes in the walls of a standard toroidal ferrite core and the passing of a current down a wire threading these holes to produce nondestructive READ.

The BIAX memory and logic devices described by Wanlass[4] both depend upon the interference of crossed magnetic fields for their operation.

Impulse switching by Newhouse[5] and the work of Rajchman,[6] Shevel,[7] Papoulis,[8] and others in the field has all led to a better understanding of the phenomena observed in cross magnetic field devices.

Write Operation

Fluxlok orthogonal WRITE, for changing the information state of word bits, involves the coincidence of what are normally READ pulse currents in the word solenoid of a memory plane (Fig. 3) and polarized information currents in the sense lines at the bit locations whose states are to be changed. Theoretically, the orthogonal magnetizing force from the interrogate pulse in the solenoid will produce a rotation of most of the magnetic moments in the cores, and the below-switching-threshold mmf from the polarized information current in the sense line will add to this magnetizing force—the effect could conceivably be sufficient to rotate the moments beyond the critical 90° point and thus, allow

[1] D. A. Buck and W. I. Frank, "Nondestructive sensing of magnetic cores," *Commun. and Electronics*, No. 10 (*AIEE Trans.*, Pt. I, vol. 72), pp. 822–830; January, 1954.

[2] U. F. Gianola, "Nondestructive memory employing a domain oriented steel wire," *J. Appl. Phys.*, vol. 29, pp. 849–853; May, 1958.

[3] R. Thorensen and W. R. Arsenault, "A new nondestructive read for magnetic core," *Proc. WJCC*, pp. 111–116; March, 1955.

[4] C. L. Wanlass and S. D. Wanlass, "Biax high speed computer element," 1959 WESCON Convention Record, pt. 4, pp. 40–54.

[5] V. L. Newhouse, "The utilization of domain wall viscosity in data handling devices," Proc. IRE, vol. 45, pp. 1484–1492; November, 1957.

[6] J. A. Rajchman and A. W. Lo, "The transfluxor," Proc. IRE, vol. 44, pp. 321–332; March, 1956.

[7] W. L. Shevel, Jr., "Millimicrosecond switching properties of ferrite computer elements," *J. Appl. Phys.*, suppl. to vol. 30, pp. 475–485; April, 1959.

[8] A. Papoulis, "Nondestructive read-out of magnetic cores," Proc. IRE, vol. 42, pp. 1283–1288; August, 1954.

em to relax to a new and opposite state of remanence. here the bits are to remain in their prior ONE or ERO state, the information current polarity is made ch as to drive the cores further into their existing manent state. Orthogonal WRITE, then, is an over-lling action in which it is not necessary to first clear l bits of a word to a reference state as in destructive re memories. Fig. 7 represents this coincident or-ogonal WRITE action, where the vector A represents e cross magnetic field from the solenoid and the ctor B represents the field produced by the informa-on current in the sense line; together they might be pected to result in an extremely fast switching of the re from one given state to the opposite state of rema-nence.

Fig. 7—Vector representation of orthogonal WRITE.

Thus, it was originally thought that the coincidence f the pulsed orthogonal solenoid field and the informa-on current mmf in the core would cause 180° realign-ent of the magnetic moments with the application of *single* pulse from what is normally the READ driver.

Investigation revealed that a core *would not* change s information state with the application of a single lenoid pulse, but that it required a series of such lenoid pulses (about 25) to fully change the informa-on state of the core. Increasing the pulse width from a ominal 0.1 μsec to several microseconds had no bene-cial effect. Similarly, it was determined that the rise ime of the solenoid pulse was not a governing factor.

Fig. 8 is a plot of laboratory data showing the effect of arying the number of solenoid pulses for a single write peration, starting in each case from a saturated ref-rence state of opposite remanence. Additional tests howed that an increase in the solonoid pulse amplitude esulted in an expected decrease in the number of pulses equired for full switching of the core.

One theory as to the mechanism by which this slow atchet-like WRITE operation takes place is concerned ith the differing effects of the pulsed solenoid cross eld on the core magnetic moments in the various egments of the core. It is obvious, referring to Fig. 9, hat the cross field opposes the direction of the rema-nence moments in the lower part of the core, while at he same time this cross field is in a direction to aid the emanence moments in the upper part of the core. Simply stated, it is reasoned that during the presence f a solenoid pulse, the flux density in the lower part of he core is decreased by the combined solenoid field nd information current core mmf, and that the flux

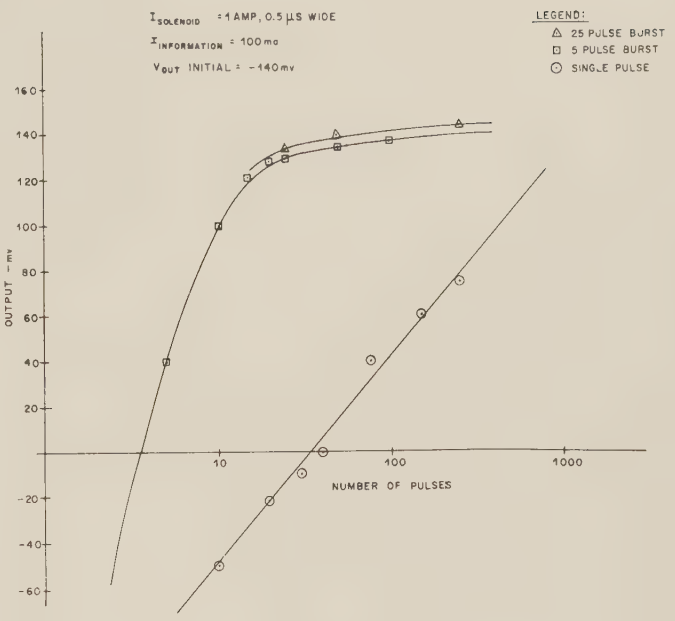

Fig. 8—Orthogonal WRITE test data.

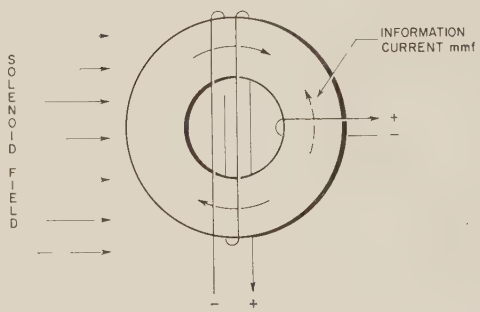

Fig. 9—WRITE action for changing state of core from ZERO (CW) to ONE (CCW).

density in the upper part of the core is changed very little, as flux changes in this part of the core are opposed by the mmf produced by the information current. Upon termination of the pulse field, the core assumes a minimum energy state wherein the two flux densities again become equal. In this case, the information current forms a decrease in the flux in the upper part and opposes an increase in the flux of the lower part. The result is that the net core flux has been reduced slightly towards a demagnetized state. Repeated applications of solenoid pulses gradually "walk" the core state through the demagnetized state and eventually to the desired opposite state of saturation.

Fluxlok Test Vehicle

The objective in constructing a laboratory test vehicle for a high-speed Fluxlok nondestructive memory was to provide a device which could demonstrate, on a continuous test basis, the reliability of the memory and the integrity of the operating theory. In the design chosen, the test vehicle can compare the contents of

the memory (by means of sequential addressing) with the contents of the binary counter performing the addressing of the memory. In addition, provision was made for setting up a comparison word on a series of switches so that any pattern could be entered into any word position and compared during the test cycling of the memory. These patterns are entered by the orthogonal field method of writing. Fig. 10 shows a block diagram of the test vehicle.

The test vehicle memory "slice," or partial stack, consisted of eight planes of eight 24-bit words each. Fig. 11 is a photograph of one of the memory planes. The storage elements were 50/80-mil ferrite cores. The unit was assembled to simulate a larger memory stack to facilitate studies of noise and crosstalk that might be encountered in a full-sized memory. The ends of the additional wires, added in parallel with the word windings for coincident current write, may be seen in the photograph.

A nominal READ rate of 2 mc, dictated by a supporting project requirement, was chosen for this test vehicle. All circuitry was transistorized except that vacuum-tube drivers were designed to furnish the high-current fast-rise-time pulses at this frequency As previously mentioned, reliable solid-state drivers to furnish one-ampere pulses with 50-nsec rise times are limited to about a 500-kc repetition rate with present-day semiconductor devices. Sense line signals were fairly clean and uniform, and the sense amplifier design has proved adequate for the fast-rise-time bipolar output signals.

Fig. 12 is an oscilloscope display of the waveforms taken. The memory vehicle was tested satisfactorily and delivered to the customer under BuShips Contract NObsr 72747.

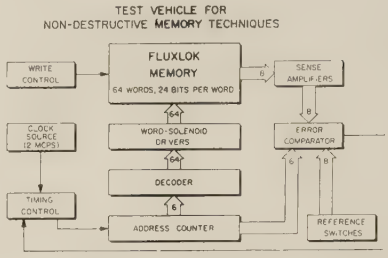

Fig. 10—Fluxlok memory test vehicle block diagram.

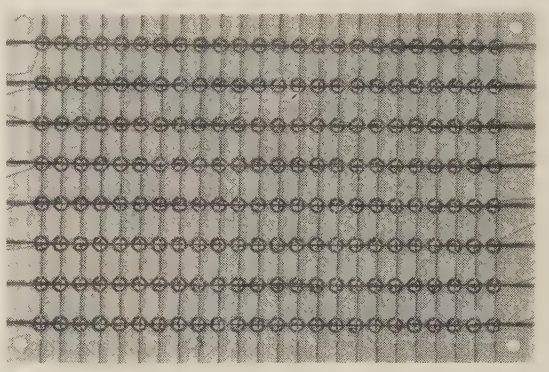

Fig. 11—Fluxlok memory plane, enlarged.

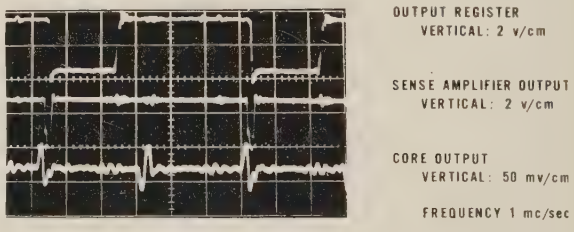

Fig. 12—Relative timing of output register, sense amplifier, and core outputs showing binary 101.

Future Development

Development of the Fluxlok memory technique is continuing. Memory READ/WRITE drivers, differential input sense amplifiers, and memory selection circuits have been designed and tested using semiconductor devices. System studies have been made and are continuing on both general-purpose and digital differential analyzer machines using the Fluxlok memory technique, where its inherent random-access and high-speed nondestructive-READ features are vital. Several large memories are being constructed for use in computer systems now under development.

Recent laboratory experiments[9] have resulted in improvements in Fluxlok operation. Read pulse power requirements have been reduced by a factor of five for the same magnitude of output signals described herein, where a one-ampere pulse was applied to a four-turn solenoid. Such a reduction of read pulse current requirements allows increased speed of the solid-state memory driver and selection circuits, further reduction in the noise factor of the memory stack, and provides an increase in the over-all reliability. Mechanical packaging techniques have been developed for the economical manufacture of large Fluxlok memory systems.

The Fluxlok memory development represents one of many techniques currently under study at the Burroughs Research Center in which principally orthogonal magnetic fields are employed in conjunction with a variety of standard and nonstandard geometrical memory and logic devices.

Acknowledgment

It is a pleasure to acknowledge the many contributions of A. J. Meyerhoff, G. H. Barnes, and R. L. Gray to the original analysis and evaluation of the Fluxlok principle, and to the engineering effort leading to the successful prosecution of this computer memory development program.

[9] The subject matter of the forthcoming article is to be submitted for publication.

Magnetostrictive Ultrasonic Delay Lines for a PCM Communication System*

D. A. AARONSON†, SENIOR MEMBER, IRE AND D. B. JAMES†, MEMBER, IRE

Summary—A servo-operated delay-line pad and a temperature-mpensated delay-line memory, both magnetostrictively driven at 5 mc, have been used in an experimental PCM communication stem.[1]

The delay-line pad automatically compensates for external delay anges as small as plus or minus 8 mμsec at a rate of 75 mμsec econd. The delay-line memory stores 192 bits which are available rially with an access time of 125 μsec. Both applications use the same sic delay lines which consist of a length of 0.003-inch diameter permendur wire, two tiny solenoids, and a supporting structure.

Introduction

An adjustable delay line and a small fast access memory were required in a research experimental integrated PCM Communication System lled ESSEX[1-3] (Experimental Solid-State Exchange). Vire magnetostrictive ultrasonic delay lines were chosen or both these jobs for economy in types of components nd because they are stable, reliable, capable of good esolution, and relatively easy and economical to build.

In the ESSEX Telephone System, subscribers' lines e connected to small time-division switching and ransmission units which are remote from the central witching and control module. In these remote units, nalog signals are multiplexed and converted to digital gnals before being transmitted and switched as PCM gnals via the central module.[2] The signals are conerted back to analog form only at the unit to which ney are directed.

The voice-frequency signals in a subscribers' line are ampled at an 8000-cps rate. The period between amples of the same message, 125 μsec, is called a *frame*. he gates at the central module, operating once per rame for each message, require that the PCM signals rom each remote unit arrive at the center module in ynchronism with the PCM signals being sent to the emote unit. Since the remote units may be located at ifferent distances from the central module, the loop ransmission time, of the order of 7 μsec/mile, must e padded to an integral number of frames. A manually-djustable magnetostrictive ultrasonic delay line inserted in the loop is well suited for this job. In addition, there are small variations in transmission time due to temperature changes in the system. For example, when the transmission is over aerial exchange cable, these temperature variations of delay are of the order of ±0.2 μsec/mile for the maximum temperature range expected.[4] A servo unit mounted on the delay line automatically compensates for this.

Fast cyclic-access circulating delay-line memories are used for controlling periodically operated switches and for recording the status of calls in progress.

The Basic Delay Line and Amplifiers

The basic magnetostrictively-driven ultrasonic wire delay line has a wider bandwith than most in common use. Electrical pulses are applied at baseband at a 1.5-mc rate by means of a transistorized blocking oscillator and driver, Fig. 1. Fig. 2 shows a typical line. It consists of a three-foot-long frame holding a 0.003-inch-diameter supermendur[5] wire, having two tiny solenoidal transducers mounted on movable carriages. Delay is adjustable from about 5 μsec to about 130 μsec. The theory and principle of operation of these lines is well described in the literature.[6] In the sending transducer, an electrical pulse is converted into acoustical energy through the magnetostrictive effect in the supermendur wire. The acoustical pulse travels along the wire at the speed of sound, which is about 5 μsec/inch for the longitudinal mode used here. At the receiving transducer, which is identical to the sending one, the acoustical pulse is converted back to an electrical pulse through the inverse magnetostrictive effect. Unwanted reflections from the ends of the supermendur wire are mechanically damped out with rubber cement. The 10-mv pulse output from the receiving transducer is amplified and reshaped by a four transistor, transformer coupled amplifier, Fig. 3, to provide a 4-volt 0.4-μsec pulse. Characteristics of the delay line are summarized in Table I.

Small permanent magnets at each transducer provide a polarizing field for optimum operation on the linear portion of the magnetostrictive characteristic of the supermendur. Annealing of the supermendur wire at

* Received by the PGEC, March 3, 1960; revised manuscript ceived May 14, 1960.

† Bell Telephone Labs., Murray Hill, N. J.

[1] H. E. Vaughan, "Research model for time-separation integrated mmunication," *Bell Sys. Tech. J.*, vol. 38, pp. 909–932; July, 1959.

[2] D. B. James and J. D. Johannesen, "A remote line concentrator r a time-separation switching experiment," *Bell. Sys. Tech. J.*, vol. , pp. 31–57; January, 1960.

[3] W. A. Malthaner and J. P. Runyon, "Controller for a remote ne concentrator in a time-separation switching experiment," *Bell ys. Tech. J.*, vol. 39, pp. 59–86; January, 1960.

[4] J. W. Suurballe, private communication.

[5] H. L. B. Gould and D. H. Wenny, "Supermendur, a new rectangular-loop magnetic material," *Elec. Engrg.*, vol. 76, pp. 208–211; March, 1957.

[6] R. C. Williams, "Theory of magnetostrictive delay lines for pulse and continuous wave transmission," IRE TRANS. ON ULTRASONICS ENGINEERING, vol. UE-7, pp. 16–38; February, 1959.

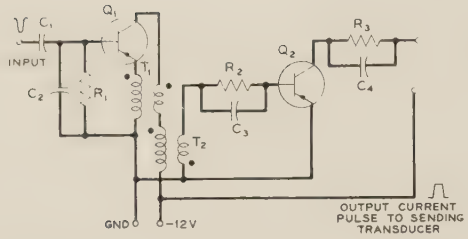

Fig. 1—Delay line driving. Amplifier: Blocking oscillator Q_1 is triggered by input pulses of 0.5 volt to 4 volts in amplitude and less than 0.3 μsec in duration. Q_2 provides almost square current pulses of up to 90 ma to the sending transducer of the delay line. Output pulse amplitude and length (about 0.3 μsec) are independent of the input pulse.

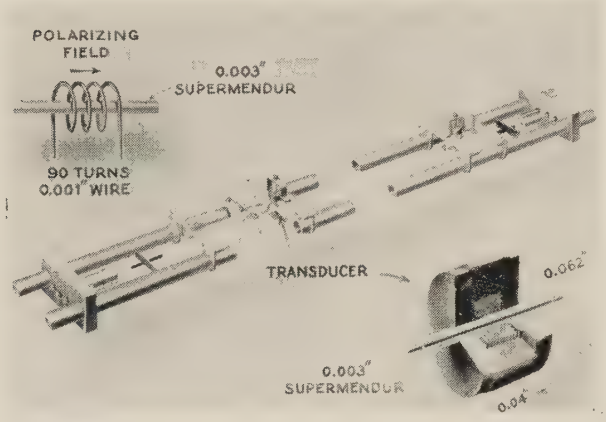

Fig. 2—Magnetostrictive ultrasonic delay line. The line consists of a frame, 3 feet long, holding a 0.003-inch-diameter supermendur wire having two solenoidal transducers mounted on movable carriages. This line is capable of delaying 1.5 megapulse per second signals up to 130 μsec.

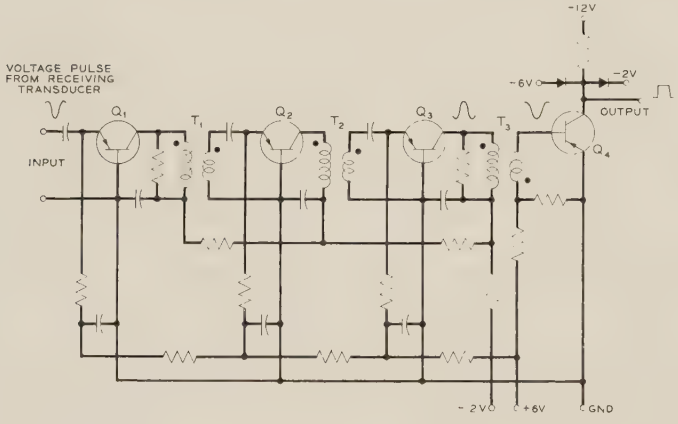

Fig. 3—Delay line receiving amplifier. The first three stages provide about 60 db of wide-band amplification for the pulse output from the delay line receiving transducer. The fourth stage, biased to cutoff, is driven into saturation by the amplified pulse. The output is clipped and clamped to give a 4-volt, 0.4-μsec pulse. Power supplies are well filtered and each stage is decoupled.

TABLE I

Characteristics of Delay Lines

Supermendur wire	
Length	~25 inches
Diameter	~0.003 inch
Transducers	
Number of turns	90
Impedance	15 to 20 ohms
Polarizing field	~100 oersteds
Driving current	75 ma

the transducers contributes up to 20 db improvement to the output signal. This improvement comes from increasing the efficiency of the transducers without significantly changing the acoustic properties of the rest of the wire.

Performance of the line is given in Table II. With the two-transistor driving amplifier and the four-transistor receiving amplifier making up for the insertion loss, we have a reliable and economical unity-gain adjustable delay line.

The Delay-Line Pad and Stabilizer Loop

A block diagram of the delay-line pad and stabilizer loop in a typical PCM channel is shown in Fig. 4. The delay line itself is included both in the transmission path from one PCM unit to another and in the stabilizing loop. At the input to the loop, the clocked slicer compares the delayed (or advanced) data pulses with reference clock pulses. The output of the clocked slicer, when rectified and integrated, is a dc error signal, whose polarity and amplitude are a function of whether the data pulses were late or early and by how much. After further dc amplification, the error signal drives a servo motor which positions the sending transducer's carriage along the delay line in the correcting direction. The specifications of the delay pad are given in Table III, below.

TABLE II

Performance of Delay Lines

Output voltage	10 mv
Output pulse width	0.4 μsec
Attenuation per 100 μsec	~3 db
Insertion loss	~50 db
Signal-to-noise ratio	~20:1

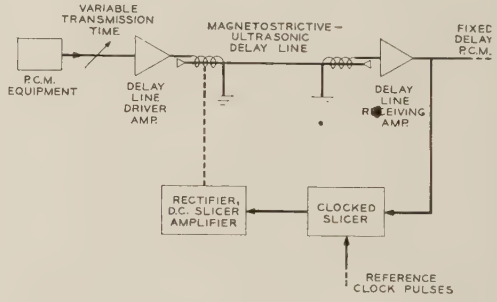

Fig. 4—Delay line pad. The pad consists of a magnetostrictive delay line in which one transducer is mounted on a driven carriage. A clocked slicer compares the time of arrival of the output pulses of the delay line with those from a reference clock, and generates a signal to move the carriage in such a direction as to maintain the constant time relation between these two sets of pulses.

TABLE III

Specifications of Delay Pads

Pulse repetition rate	1.536 mc
Delay correction limit	±8 mμsec
Rate of correction	75 mμsec/second

Fig. 5 shows the basic delay discriminator, the clocked cer. Its operation may be described in terms of the ree cases illustrated; namely, data pulses locked in, ta pulses late, or data pulses early. The base of ansistor Q_3 is held at a fixed bias so that with no coming data pulses at A, all three transistors are nconducting. Q_1 then acts as a current gate when its se is pulsed negatively, allowing either Q_2 or Q_3, but t both together, to conduct. When Q_2 conducts, Q_3 biased off, and vice versa.

In the first case, with data pulses locked in, when a ta pulse at A arrives exactly one-half a pulse width ead of the reference clock pulse at B, Q_3 is first turned for this one-half pulse time. When the clock pulse rives at Q_2, with Q_1 still on, it turns Q_2 on, which ases Q_3 off for the remaining half pulse time. We thus tain equal and opposite pulses at C and D, which add to a zero dc error at E.

If the data pulse arriving at input A is late, the second se, then Q_3 remains on for a longer period and Q_2 a orter period so that the output pulse at Q_3's collector increased in width at the expense of that at Q_2's collector. The resulting net positive dc delay error at E uses a decrease in the acoustical length of the delay ne to correct for this. Conversely, when the data pulse t input A is early, the third case, the output pulse at $_2$'s collector, is increased in width at the expense of at at Q_3, giving a net negative delay error at E. This auses an increase in the acoustical length of the delay ne to correct for this. Although idealized square pulses re illustrated, the same principle of operation holds for he actual pulses occurring in the system.

Two diode rectifiers and simple RC smoothing inteate the pulse-to-pulse error. DC slicer amplifiers, imilar in principle to the clocked slicer, provide ufficient gain to operate a reversible on-off servo, drivng the sending transducer carriage along the delay ne.

The stability of this nonlinear on-off type servo is dequate for the rather slow or long period temperature ariations of delay expected. The gain limitations were ot so severe as those of a continuous type servo,[7] and he phase margin was sufficiently large because of the c coupling used throughout the loop.

The Delay Line Memory

The same basic delay lines are also used as circulating nemories, as indicated in the composite block diagram f Fig. 6. This type of memory was chosen in preference o other storage systems such as magnetic drums or ape loops, magnetic cores, twistors, barrier grid stores, tc., because we required serial cyclic access at 1.5 mc f about 600 bits of information. The other cyclic access tores were too slow or uneconomical; most of the reaining types were either too slow or not economical

[7] L. A. MacColl, "Fundamental Theory of Servo-Mechanisms," . van Nostrand Co., Inc., Princeton, N. J., 1945.

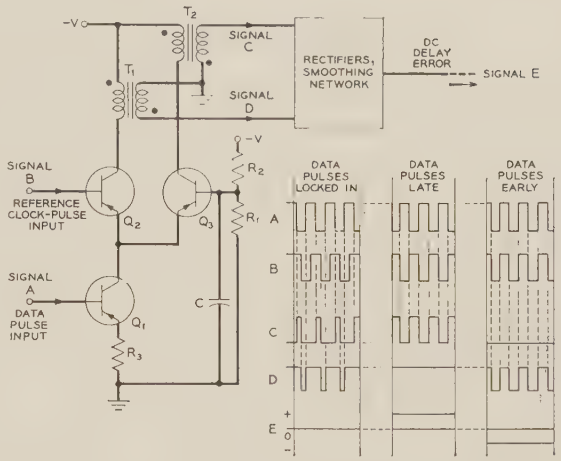

Fig. 5—Clocked slicer. This circuit divides the incoming data pulses according to whether they are in synchronism with, late, or early with respect to reference clock pulses; it generates signals which, after rectification and smoothing, can be used to vary the position of the movable transducer on the delay line. Idealized waveforms of the slicing action are shown.

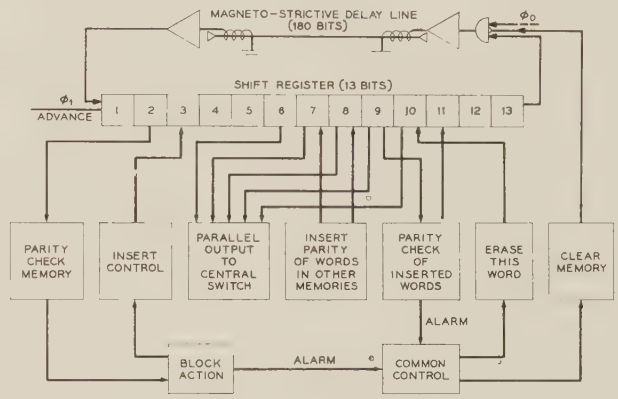

Fig. 6—Delay line memory. The memory consists of a 13-bit shift register and re-entrant magnetostrictive delay line of 180 bits in length (2 feet). The shift register allows the circulating bits to be read, checked, changed, and erased as they pass through.

in access circuitry until the number of bits reached about 10,000, or they were both too slow and uneconomical.

Each memory consists of a magnetostrictive delay line, driving and receiving amplifiers, and a 13-stage shift register operating at 1.5 mc. The line plus shift register contains 192 bits divided into 24 time slots of 8-bit words each. The 24 time slots make up one *frame* in the system. Stored 8-bit words needed in cyclic order are read out in parallel as they pass through the shift register.

Stage 1 is used to insert bits from the delay line into the register, and these are advanced to the next stage one-half a bit time later.

Stage 2 drives a serial parity check circuit to detect errors. If an error occurs, an alarm is sent out to the master or common control, and action in that time slot is blocked.

Stage 3 is used to insert new words at the half bit time from common control. Stages 6 through 10 are used for parallel readout of a 5-bit word in one case, where the

remaining 3 bits are parity bits for this word and for two other words in separate memories.

Stages 7 and 8 are used to insert the parity bits of the words of two other memories.

Stage 9 allows the serial readout of the whole 8-bit word and checks the parity of the inserted word. If an error occurs on insertion, an alarm signal is sent out asking for a second insertion trial and the time slot is blocked by making the over-all parity of all three memories incorrect.

Stage 10 is used to erase a single word.

Stage 13 is used for reading into the magnetostrictive delay line at the one-half bit time. A clear signal can be used to inhibit the delay line driver and clear the memory.

The delay lines used in this memory application are of fixed acoustical length. Any variation in acoustical length due to changes in ambient temperature are compensated for by the motion of one of the transducers, controlled by a mechanical differential expansion scheme.

Specifications of the memory line are summarized in Table IV.

TABLE IV
SPECIFICATIONS OF MEMORY LINES

Bit rate	1.536 mc
Capacity	192 bits
Access cycle	125 μsec
Output	parallel or serial

An experimental line operating at 4.5 mc has been built and could have been used instead of three of the 1.5 mc memory lines. However, this would have required that the three associated shift registers be all of the same length and that fast commutator switches be used to multiplex and demultiplex the three signals, with an over-all loss of economy.

APPLICATION AND PERFORMANCE

In the research experimental system, 12 delay line are used, three for delay pads and nine for memory functions. The 12 lines have been operating reliably i a working system for about 2 years.

Although the delay stabilizer can detect changes i transmission time as small as 8 mμsec, it is usually se to maintain the delay error within ±15 mμsec at a correction rate of 75 mμsec/second. It has satisfactorily corrected for slow and fast room temperature changes o delay of the order of 0.1 μsec in the delay line itself This is a reasonable test of the behavior expected fron exchange cable pairs.

CONCLUSION

Magnetostrictive ultrasonic delay lines have bee used in a PCM Communication System, both as delay line pads and as small temperature-compensated cir culating memories. The delay-line pad can correct fo pulse delays as small as 8 mμsec; the delay-line memorie have a capacity of 192 bits. Reliable operation witl solid-state equipment at repetition rates of 1.5 mc ha been demonstrated over a period of about 2 years. Th construction of the lines is relatively simple and eco nomical. Their physical size can be quite small. Operat ing characteristics are stable over a wide temperatur range. Use of delay lines in pulsed circuits has bee demonstrated at 1.5 and 4.5 mc.

ACKNOWLEDGMENT

The successful design of magnetostrictive ultrasoni delay lines operating at repetition rates above 1.5 m is due in great part to J. F. Muller and his group, an J. H. McGuigan. The suggestions and encouragemen of W. A. Malthaner, and H. E. Vaughan contribute much to this work. Many thanks are due also to ou associates in the Systems Research Department for th design of the solid-state delay-line amplifiers.

Error Detecting and Correcting Binary Codes for Arithmetic Operations*

DAVID T. BROWN†

Summary—The most important property of the codes derived in is paper is that two numbers, i and j, have coded forms, $C(i)$ and $j)$ that when added in a conventional binary adder, give a sum $i)+C(j)$ that differs from $C(i+j)$, the code for the sum, by (at ast) an additive constant. This makes possible the detection and/or rrection of errors committed by the arithmetic element of a com-ter. In addition, messages can be coded and decoded and errors n be detected and corrected by arithmetic procedures, making it ssible to eliminate some or all of the special-purpose equipment ually associated with error-detecting or correcting codes. This operty may make these codes useful for data transmission as well for computation.

Introduction

THE CODES to be considered are of the form $An+B$ where n is the number to be coded and A and B are constant positive integers. These odes are useful because two coded numbers can be dded and the result will differ from the coded sum ily by a constant.

$$Aj + B + Ak + B = A(j + k) + 2B. \qquad (1)$$

Certain requirements must be satisfied by an $An+B$ ode. The minimum distance between messages must e two for error detection, or three for error correction; nd the complement of a coded number in the number ase being used must be obtainable simply by comple-enting each binary symbol in the code message. This tter is necessary to facilitate subtraction.

The maximum value of n, the number to be coded, etermines the number base. Thus we can do decimal rithmetic if $n=0, 1, 2, \cdots, 9$, and each digit will have rror detection or correction. Codes can be found for an rbitrary base, but special attention will be paid to ases that are powers of two or powers of ten because hese are most convenient for translation. One exception o this exists. If a code is used with a base greater than he largest number that will occur, only a single digit eed be considered. In this case, the extact value of the ase is not important (as long as it is large enough). ingle-digit representation has some attractive features hich will be mentioned later.

Constraints on $An+B$ Codes

This section will develop the conditions that must e met for a code to have various properties. The fol-owing is a list of symbols that will be used. Throughout his paper all variables are restricted to positive in-egers.

i, j Two of the numbers to be coded; $i>j$.

$d(i, j)$ The distance between the code messages $Ai+B$ and $Aj+B$; *i.e.*, the number of binary symbol positions in which the binary representations of $Ai+B$ and $Aj+B$ differ.

r $i-j$; $r=1, 2, 3, \cdots, b-1$

b The number base. The largest number is $b-1$.

g The code length or number of binary symbols in the code message.

k, l Binary-symbol positions in the code message. The lowest order position is position zero.

Requirement for Complementation

To insure that the complement of a number can be obtained by simply complementing each bit of the code, we can write the following equation.

$$An + B + A[(b - 1) - n] + B = 2^g - 1$$

or

$$A(b - 1) + 2B = 2^g - 1, \qquad (2)$$

that is, the code for a number and the code for its complement must sum to "all ones."

Note that this equation will be satisfied only for odd values of A and even values of b. We will consider only codes for which (2) is satisfied.

Conditions for an $An+B$ Code to be Capable of Error Detection or Error Correction

The following two theorems define sufficient conditions for a code to have $d(i, j)\geqq 2$ and thus be capable of detecting all single errors, and for a code to have $d(i, j)\geqq 3$ and thus be capable of correcting all single errors.

Theorem 1: If A is odd, $\neq \pm 1$, then $d(i, j)\geqq 2$ for all $i\neq j$.

Proof: If $d(i, j)=1$ then $(Ai+B)-(Aj+B)=2^k$ because binary numbers differing in one digit differ by a power of two. Let $i-j=r$. (A positive r imposes no restriction because of the symmetry of the problem.) Now

$$r = \frac{2^k}{A}.$$

For r an integer and A an odd integer, the only solution is with $A=1$.

As we have taken $A\neq 1$ then $d(i, j)\neq 1$. If $i\neq j$ then $d(i, j)>1$, therefore $d(i, j)\geqq 2$.

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Theorem 2: If A is odd, $\neq 1$, and if $i, j < r_{min}$ with $i \neq j$, then $d(i, j) \geqq 3$ where r_{min} is the least positive integer that satisfies

$$r_{min} = \frac{2^k \pm 1}{A}. \tag{3}$$

Proof: If $d(i, j) = 2$ and we take $i > j$ then $(Ai+B) - (Aj+B) = A(i-j) = 2^k \pm 2^l$ with $k > l$. Now

$$i - j = \frac{2^k \pm 2^l}{A} = \frac{(2^{k-l} \pm 1)2^l}{A}.$$

As A is odd, it must divide the factor $2^{k-l} \pm 1$. Then it follows from the definition of r_{min} that

$$\frac{2^{k-l} \pm 1}{A} \geqq r_{min}.$$

Therefore, $i - j \geqq r_{min}\ 2^l$ to have $d(i, j) = 2$. If we take $i, j < r_{min}$, then $i - j < r_{min} \leqq r_{min}\ 2^l$ so $d(i, j) \neq 2$. From Theorem 1, $d(i, j) \geqq 2$, so $d(i, j) \geqq 3$.

The Derivation of Error Detecting Codes

From Theorem 1, the smallest value of A to guarantee single-error detection is $A = 3$. Error detecting $An+B$ codes in which $A = 3$ will have the least possible redundancy, but it is conceivable that a larger value of A could be useful because of special characteristics of the resulting code.

Table I gives $3n+B$ codes of minimum length for bases which are powers of two and powers of ten. The minimum length is the minimum value of g that satisfies [from (2)]

$$A(b - 1) \leqq 2^g - 1. \tag{4}$$

After g is determined, B can be found from (2). It can be shown that with $A = 3$ and a minimum value for g, codes will have from one to three redundant bits. This can be seen to be true in Table I as there are g total bits and b different messages, thus, $g - \log_2 b$ redundant bits.

The $3n+2$ code in Table I and the $27n+6$ code in Table III have been previously reported,[1] but all other codes given here appear to be new.

The Derivation of Error-Correcting Codes

Table II, which is based on Theorem 2, gives data for determining codes with $d(i, j) \geqq 3$. For a given A, a code can be constructed with any base less than or equal to the r_{min} associated with that A.

Table III lists single-error-correcting codes for bases which are powers of two and powers of ten. Codes of minimum length are listed for each base. The codes were determined according to the following procedure.

[1] R. M. Diamond, "Checking codes for digital computers," Proc. IRE, vol. 43, pp. 487–488; April, 1955.

TABLE I

Minimum Length Single Error Detecting $3n + B$ Codes

Base—b	Length—g	Code
10	5	$3n + 2$
100	9	$3n + 107$
1000	12	$3n + 549$
10000	15	$3n + 1385$
2	2	$3n + 0$
4	4	$3n + 3$
8	5	$3n + 5$
16	6	$3n + 9$
32	7	$3n + 17$
64	8	$3n + 33$
128	9	$3n + 65$
256	10	$3n + 129$
512	11	$3n + 257$
1024	12	$3n + 513$

TABLE II

Data for Single Error Correcting $An+B$ Codes

A	min $(2^k \pm 1) = Ar_{min}$	r_{min}
3	$2^1 + 1$	1
5	$2^2 + 1$	1
7	$2^3 - 1$	1
9	$2^3 + 1$	1
11	$2^5 + 1$	3
13	$2^6 + 1$	5
15	$2^4 - 1$	1
17	$2^4 + 1$	1
19	$2^9 + 1$	27
21	$2^6 - 1$	3
23	$2^{11} - 1$	89
25	$2^{10} + 1$	41
27	$2^9 + 1$	19
29	$2^{14} + 1$	565
31	$2^5 - 1$	1
33	$2^5 + 1$	1
35	$2^{12} - 1$	117
37	$2^{18} + 1$	7085
39	$2^{12} - 1$	105
41	$2^{10} + 1$	25
43	$2^7 + 1$	3
45	$2^{12} - 1$	91
47	$2^{23} - 1$	178481
49	$2^{21} - 1$	42799
51	$2^8 - 1$	5
53	$2^{26} + 1$	1266205
55	$2^{20} - 1$	19065
57	$2^9 + 1$	9
59	$2^{29} + 1$	9099507
61	$2^{30} + 1$	17602325
63	$2^6 - 1$	1
65	$2^6 + 1$	1
67	$2^{33} + 1$	128207979
69	$2^{22} - 1$	60787
71	$2^{35} - 1$	483939977
73	$2^9 - 1$	7
75	$2^{20} - 1$	13981
77	$2^{30} - 1$	13944699
79	$2^{39} - 1$	6958934353
81	$2^{27} + 1$	1657009
83	$2^{41} + 1$	26494256091
85	$2^8 - 1$	3
87	$2^{28} - 1$	3085465
89	$2^{11} - 1$	23
91	$2^{12} - 1$	45
93	$2^{10} - 1$	11
95	$2^{36} - 1$	723362913
97	$2^{24} + 1$	172961
99	$2^{15} + 1$	331
101	$2^{50} + 1$	5099523830125
103	$2^{51} - 1$	11350134113449

TABLE III

SINGLE ERROR CORRECTING $An + B$ CODES OF MINIMUM LENGTH

Base	Length	Codes	
10	8	$19n + 42$ $25n + 15$	$23n + 24$ $27n + 6$
100	12	$29n + 612$ $37n + 216$	$35n + 315$ $39n + 117$
1000	16	$37n + 14286$ $49n + 8292$ $55n + 5295$ $61n + 2298$	$47n + 9291$ $53n + 6294$ $59n + 3353$
2	3	$7n + 0$	
4	6	$13n + 12$ $21n + 0$	$19n + 3$
8	8	$19n + 61$ $25n + 40$ $29n + 26$	$23n + 47$ $27n + 33$ $35n + 5$
16	9	$19n + 113$ $25n + 68$ $29n + 38$	$23n + 83$ $27n + 53$
32	10	$23n + 155$ $29n + 62$	$25n + 124$
64	11	$23n + 279$	$29n + 110$
128	12	$29n + 206$	
256	13	$29n + 398$	
512	14	$29n + 782$	
1024	16	$37n + 13842$ $49n + 7704$ $55n + 4630$ $61n + 1566$	$47n + 8727$ $53n + 5658$ $59n + 2645$

1) Find the smallest A for which $r_{\min} \geqq b$
2) Use this A in (4) to find g
3) Use (2) to find B
4) Repeat for the next larger A for which $r_{\min} \geqq b$ until g becomes larger.

Table IV gives the coded messages for the minimum-distance base-ten codes.

CODES WITH $B = 0$

If two coded numbers are added, the sum must generally be adjusted in each digit to achieve the correct code for the sum. This correction is a result of two factors. First, when $Ai+B$ and $Aj+B$ are added the sum is greater than $A(i+j)+B$ by the constant B. Second, when carries exist between the coded digits, legal code words do not result; so an adjustment is necessary depending on the carry in to a digit and the carry out of a digit. (The patterns to implement these adjustments are given in Appendix I.) The corrections can be quite readily implemented, but where speed is a vital factor the necessity of correction is a definite drawback.

Corrections can be eliminated if a code is chosen with $B = 0$ and a base larger than any number that ever will be encountered. All numbers will be represented by a single digit eliminating interdigit carries, and the sum of two code messages will be the code for the sum.

It is possible to find many error-detecting codes with $B = 0$ and a large base by employing (2) with B set equal to zero.

$$A(b - 1) = 2^g - 1. \tag{5}$$

TABLE IV

$An + B$ CODES WITH BASE 10, MINIMUM DISTANCE 3, AND LENGTH 8

Character	$19n + 42$ Message	Decimal Equivalent	Character	$23n + 24$ Message	Decimal Equivalent
0	0 0 1 0 1 0 1 0	42	0	0 0 0 1	
1	0 0 1 1 1 1 0 1	61	1	0 0 1 0 1 1 1	
2	0 1 0 1 0 0 0 0	80	2	0 1 0 0 0 1	
3	0 1 1 0 0 0 1 1	99	3	0 1	
4	0 1 1 1 0 1 1 0	118	4	0 1 1 1	
5	1 0 0 0 1 0 0 1	137	5	1 0 0 0	
6	1 0 0 1 1 1 0 0	156	6	1 0	
7	1 0 1 0 1 1 1 1	175	7	0	
8	1 1 0 0 0 0 1 0	194	8	1	
9	1 1 0 1 0 1 0 1	213	9	1	
Character	$25n + 15$ Message	Decimal Equivalent	Character		
0	0 0 0 0 1 1 1 1	15	0		
1	0 0 1 0 1 0 0 0	40	1		
2	0 1 0 0 0 0 0 1	65	2		
3	0 1 0 1 1 0 1 0	90	3		
4	0 1 1 1 0 0 1 1	115	4		
5	1 0 0 0 1 1 0 0	140	5		
6	1 0 1 0 0 1 0 1	165	6		
7	1 0 1 1 1 1 1 0	190	7		
8	1 1 0 1 0 1 1 1	215	8		
9	1 1 1 1 0 0 0 0	240	9		

The situation is different for error-correcting codes, however.

From (5)

$$b - 1 = \frac{2^g - 1}{A}.$$

From this requirement, and by the definition of $r_{\min}$, $b-1 \geqq r_{\min}$, no $B=0$ code can satisfy Theorem 2. However, the converse of Theorem 2 is not true. Theorem 3 states that under certain conditions a $d(i, j) \geqq 3$ code can contain numbers up to and including $r_{\min}$.

Theorem 3: If $(A)\ (r_{\min}) = 2^k - 1$, the $B=0$ code with a base $b = r_{\min} + 1$ has $d(i, j) \geqq 3$.

Proof: From the proof of Theorem 2, $d(i, j) \geqq 3$ if $i - j < r_{\min}$. The only pair for which this does not hold is $r_{\min}$, 0. Because $B=0$, $d(r_{\min}, 0)$ is equal to the number of positions in $(A)\ (r_{\min})$ containing a one. $(A)\ (r_{\min}) = 2^k - 1$ so $(A)\ (r_{\min})$ contains k ones and from Table II, $k \geqq 3$.

For example, from Table II we see that the code $71n$ has $d(i, j) \geqq 3$. The messages are 35 binary symbols long and the largest number that can be coded is 483,939,977. There are $35 - \log_2 483{,}939{,}977 = 6.15$ bits of redundancy. By comparison, a 35-digit Hamming code[2] has 6 bits of redundancy.

Error Detection and Correction

The most obvious method of error detection is to subtract B from a received message and divide by A. The remainder will be zero if and only if no single errors have been committed. This method could be used if it were desired to eliminate special error-detecting equipment and use general-purpose equipment for detection. B need not be subtracted if the test is made for the residue B (mod A) instead of for zero.

The above detection procedure requires a division [illegible] is expensive in time. Theorem 4 gives a method [illegible] the residue of a number (mod 3) without providing a fast means of error detec-

[illegible] (mod 3) of a binary-coded

[illegible] (mod 3)

[illegible] ectively the number of [illegible] nd the number of ones

[illegible] r be

[illegible] $D_1 2^1 + D_0$

[illegible] refore

[illegible] (mod 3),

[illegible] ing codes,"

hence

$$D_{g-1}2^{g-1} + D_{g-2}2^{g-2} + \cdots + D_1 2^1 + D_0 \equiv D_0 - D_1 + D_2 - D_3 + \cdots \pmod{}$$

proving the theorem.

This theorem can be implemented by a combinatori circuit of reasonable size.

Error correction can be performed by dividing a r ceived $d(i, j) \geqq 3$ code message by A, as indicated b Theorem 5.

Theorem 5: An $An+B$ code message with $d(i, j) \geqq$ will give a unique residue (mod A) for every possib single error and for no error.

Proof: An $An+B$ code message that may or may n contain a single error will be of the form

$$Ai + B \pm 2^k \qquad k = -\infty, 0, 1, 2, \cdots g-1.$$

Assume

$$Ai + B \pm 2^k \equiv Ai + B \pm 2^l \pmod{A} \qquad k > l.$$

All four combinations of sign are allowed.

$$\pm 2^k \equiv \pm 2^l \pmod{A}$$
$$\pm 2^k \pm 2^l \equiv 0 \pmod{A}.$$

From this it follows that for some i, j

$$Ai + B \pm 2^k \pm 2^l = Aj + B.$$

This implies that by changing less than three dig in a code message, we can achieve another legal messag This is contrary to the restriction $d(i, j) \geqq 3$. Hence t assumption is false and the theorem is proved.

Given a residue, the position in error can be found b a table lookup procedure or by the arithmetic procedu outlined in Appendix II.

From the proof of Theorem 5 it follows that certa multiple errors can be corrected. If a received messa differs from the true message by $\pm 2^k$, k can be dete mined and so the true message can be found. Thus can correct not only single errors, but also any err pattern that corrupts the true message by a power two.

For example:

True message 0 1 1 1 0 1 1 0 = 19(4) + 42 from t $19n+42$ code. Received message 1 0 0 0 0 1 1 0 = tr message + 2^4.

Theorem 5 proves that this received message can corrected although it differs from the true message four positions. Correction of this type of error patte would be useful in an adder as it corresponds to a fau in a carry.

A particularly useful type of error-correcting code h an A that contains a factor of three. With this situatio errors can be efficiently detected by implementi Theorem 4. It is then necessary to divide by A a examine the residue only when an error actually occu

ecause errors are assumed to be infrequent, the time quired to divide is unimportant. With this method, special-purpose error-correcting equipment (which ould stand idle most of the time) is required; yet the st in time is small.

Conclusions

Sufficient conditions for an $An+B$ code to have ngle-error detection or single-error correction have en developed. In addition, some special types of des such as codes with $B=0$ or with A containing a ctor of three were presented. There are undoubtedly any other constraints that may be placed on these des to benefit particular applications.

Acknowledgment

The author is indebted to J. E. MacDonald who proosed a study of this type of code and has made many elpful suggestions during the course of the work.

Appendix I

Corrective Add Patterns for Addition Employing $An+B$ Codes

Consider two multidigit numbers with each digit oded in the form $An+B$. If these two numbers are dded in a conventional binary adder, a corrective addion must be performed after the regular addition to chieve the correct sum in coded form. The correction o each digit depends only on the carry in to and the arry out of that digit during the regular addition and, f course, on the particular code employed.

In particular:

1) The sum of two coded digits is greater than the code for the sum by the amount B.
2) A carry in to a digit should add A to the digit. Without correction it would add only one.
3) A carry out of a digit should subtract Ab from the digit. Without correction it subtracts 2^g.

It should be noted here that when two coded digits hose sum is greater than $b-1$ are added, there will be carry out of the high-order position during the regular ddition. It now follows that we should trap the interigit carries during regular addition and use them to etermine the corrective add pattern.

The general corrective add patterns can now be ritten.

During Regular Addition		Preliminary Sum	Corrective Add Pattern
C_{in}	C_{out}		
0	0	$A(i+j)+2B$	$-B$
1	0	$A(i+j)+2B+1$	$A-B-1$
0	1	$A(i+j)+2B-2^g$	2^g-Ab-B
1	1	$A(i+j)+2B-2^g+1$	$2^g-Ab+A-B-1$

If a corrective add pattern is a negative number, its complement can be formed by adding 2^g. Thus, the corrective add pattern for $C_{in}=C_{out}=0$ becomes 2^g-B.

Interdigit carries must be blocked during the corrective addition cycle.

Appendix II

A Procedure for Finding the Position in Error

The following example illustrates a procedure that could be used to determine the position in error in a code message. First B is subtracted and then a division is performed to determine the residue (mod A).

$$Ai + B \pm 2^k - B \equiv \pm 2^k \pmod{A}.$$

For example, let $A=23$.

k	$+2^k \pmod{23}$	$-2^k \pmod{23}$
0	1	22
1	2	21
2	4	19
3	8	15
4	16	7
5	9	14
6	18	5
7	13	10
8	3	20
9	6	17
10	12	11

Note that either each residue is twice the residue above it or it is odd; also note that each row has one odd and one even number, the sum of which is 23.

The problem is, given a residue, to find k, the position in error. We proceed by the following rules.

1) Divide the residue by two until the quotient is odd.
2) Subtract this number from 23 yielding the even number in the other column.
3) Repeat the above steps until a quotient of 22 is achieved. Count the number of divisions. This is equal to k.

A Theorem for Deriving Majority-Logic Networks Within an Augmented Boolean Algebra*

R. LINDAMAN†

Summary—**Recent developments in computer technology have produced devices (parametrons, Esaki diodes) that act logically as binary majority-decision elements. Conventional design techniques fail to utilize fully the logical properties of these devices. The resulting designs are extravagant with respect to the number of components used and the operating time required. This paper reviews the conventional technique briefly and proposes an alternative method that produces more nearly minimal designs.**

Introduction

A BINARY majority-decision element is, by definition, a device that accepts several binary inputs and produces binary outputs that are determined by the majority of the inputs. The discussion that follows is limited to three-input, one-output devices in which the output agrees with the majority of the inputs. That is, the output is "1" if and only if at least two of the inputs are "1"s.

Since ordinary Boolean algebra provides no single symbol to denote the majority-decision operation, ordinary Boolean equations can not, in general, directly represent majority-decision networks. This fact leads to the alternatives of either 1) restricting the majority-decision operators to what can be represented by ordinary Boolean algebra, or 2) augmenting Boolean algebra with new notation to represent the majority-decision operation.

Conventional Design Method

The first alternative, that of restricting majority-decision networks so that they can be treated by ordinary Boolean algebra, is the basis of the conventional design method.[1] This method depends on the fact that unconditional inputs reduce majority elements to AND's and OR's. That is, an input that is always "1" reduces a three-input majority element to an OR, and an input that is always "0" reduces a three-input majority element to an AND. This method permits use of familiar design techniques but produces extravagant designs.

Majority-Logic Design Method

The second alternative, that of augmenting Boolean notation so that the majority-decision operation can be directly represented, is the basis of the design method introduced in this paper.[2] This new method is, at least in principle, capable of producing minimal designs, but requires the development of new logical formalism, theorems, etc.

The proposed notation for the majority element is paired "#"s; that is

$$A \# B \# C \equiv AB + AC + BC. \tag{1}$$

The utility of this notation is suggested by an example in which A, B, and C are the addend, augend, and low-order carry inputs to a stage of a full binary adder. The network required to produce the carry output, K, is given in ordinary Boolean notation by

$$K = C(A + B) + \overline{C}(A \cdot B), \tag{2}$$

which corresponds to five two-input AND's and OR's. That is, (2) describes a network of five three-input majority-decision elements, all with unconditional inputs. Conventional Boolean simplifications reduce the number of decision elements to four, as indicated by

$$K = C(A + B) + AB. \tag{3}$$

Fig. 1 is a diagram corresponding to (3). Each of the four D-shaped graphic symbols represents a three-input majority-decision element. The two squares labeled "D" represent one-cycle delays required to synchronize inputs to the majority elements. The upper input to each element is an unconditional "1" that reduces the three-input majority element to a two-input OR or AND. The AND is produced only if the unconditional "1" is negated (small circle) to become an unconditional "0" input.

Conventional design permits no further simplification of the network of Fig. 1. Comparison of (3) and (1), however, reveals that only one majority-decision ele-

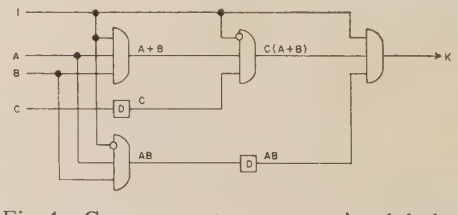

Fig. 1—Carry generator—conventional design.

* Received by the PGEC, January 15, 1960; revised manuscript received, May 10, 1960.

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[1] R. L. Wigington, "A new concept in computing," Proc. IRE, vol. 47, pp. 516–523; April, 1959.

[2] This method is adumbrated by R. Lindaman in "A new concept in computing," Proc. IRE, vol. 48, p. 257; February, 1960.

ient is required to produce the carry output; that is

$$K = A \# B \# C. \tag{4}$$

Fig. 2 is a diagram corresponding to (4). In one sense (3) and (4) are equivalent, but they differ in that (4) represents a network (Fig. 2) that requires a fourth as many components and a third the operating time of the network represented by (3) (Fig. 1). "Operating time" denotes the delay between receipt of inputs and production of outputs. It is directly proportional to the number of component columns on the logic diagram.

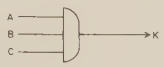

Fig. 2—Carry generator—majority-logic design.

Conversion Theorem

The above paragraph gives the simplest possible example of the advantages of majority-element notation. The translation from (3) to (4) is trivial and, indeed, (4) is itself self-evident. In general, however, design equations do not assume majority form so easily. The introduction of the "#" must be supported by rules for its use and especially by methods of converting ordinary Boolean equations into majority-element form. Such a conversion method is embodied in the following theorem:

$$X \sum_{i=1}^{n-1} f_i + \overline{X} \prod_{i=n}^{2n-2} f_i = m_n[X, (Xf_1 + \overline{X}f_n), (Xf_2 + \overline{X}f_{n+1}), \cdots, (Xf_{n-1} + \overline{X}f_{2n-2})], \tag{5}$$

where

$$m_n(V_1, V_2, \cdots, V_n) \equiv V_1 \# [m_{n-1}(V_1, \cdots, V_{n-1})] \# V_n \tag{6}$$

and

$$m_3(V_1, V_2, V_3) \equiv V_1 \# V_2 \# V_3. \tag{7}$$

It is understood that all sums, products, etc. indicated in (5), (6), and (7) are logical operations. The X's and V's represent Boolean literals, the f's represent functions of Boolean literals other than X, n represents the number of independent Boolean literals in the given equation, and m_n represents a function that is defined recursively by (6) and (7). The expression to be converted is first rewritten in the form of the left-hand side of (5). Ordinary Boolean manipulations make this possible. The right-hand side of (5) is then the converted form. The converted form is usually simpler than the original because each "#" in the converted form corresponds to from two to five AND's and OR's of the original form.

A proof of theorem (5) is given in the final section of this paper.

Sample Problems

Interpretation of theorem (5) is clarified by three examples for $n=3$ and one for $n=4$.

The first step in applying theorem (5) to any problem is to reduce it to a more special form by replacing n by its numerical value. For $n=3$, it becomes

$$X \sum_{i=1}^{2} f_i + \overline{X} \prod_{i=3}^{4} f_i = m_3[X, (Xf_1 + \overline{X}f_3), (Xf_2 + \overline{X}f_4)]$$

$$X(f_1 + f_2) + \overline{X}f_3f_4 = X \# (Xf_1 + \overline{X}f_3) \# (Xf_2 + \overline{X}f_4). \tag{8}$$

The first $n=3$ example is a three-bit parity checker (which could by iteration become a larger parity checker). Since an even-parity code conventionally represents an error, a three-bit parity error detector is given by

$$E = AB\overline{C} + A\overline{B}C + \overline{A}BC + \overline{A}\,\overline{B}\,\overline{C}. \tag{9}$$

Arbitrarily selecting A as X (any other choice would serve as well), we factor (9) to obtain

$$E = A(B\overline{C} + \overline{B}C) + \overline{A}(BC + \overline{B}\,\overline{C}). \tag{10}$$

Conversion of (10) to form (8) is completed by expressing $BC + \overline{B}\,\overline{C}$ as a product to give

$$E = A(B\overline{C} + \overline{B}C) + \overline{A}(B + \overline{C})(\overline{B} + C). \tag{11}$$

Comparison of (11) with (8) shows $A=X$, $B\overline{C}=f_1$, $\overline{B}C=f_2$, $B+\overline{C}=f_3$, and $\overline{B}+C=f_4$. Application of (8) yields

$$E = A \# (AB\overline{C} + \overline{A}B + \overline{A}\,\overline{C}) \# (A\overline{B}C + \overline{A}\,\overline{B} + \overline{A}C). \tag{12}$$

Application of (8) to the two parentheses of (12) yields

$$E = A \# (\overline{A} \# B \# \overline{C}) \# (\overline{A} \# \overline{B} \# C), \tag{13}$$

which represents a three-element network, whereas conventional design from (10) requires nine elements.

The second $n=3$ example is completion of the design of a stage of a full binary adder. The carry output is given by (4); the sum output is given by

$$\begin{aligned} S &= A(BC + \overline{B}\,\overline{C}) + \overline{A}(B\overline{C} + \overline{B}C) \qquad (14)\\ &= A(BC + \overline{B}\,\overline{C}) + \overline{A}(B + C)(\overline{B} + \overline{C})\\ &= A \# (ABC + \overline{A}B + \overline{A}C) \# (A\overline{B}\,\overline{C} + \overline{A}\,\overline{B} + \overline{A}\,\overline{C})\\ &= A \# (\overline{A} \# B \# C) \# (\overline{A} \# \overline{B} \# \overline{C})\\ &= A \# (\overline{A} \# B \# C) \# \overline{K}, \qquad (15) \end{aligned}$$

which represents a three-element network (Fig. 3),[3] whereas conventional design requires eight elements (Fig. 4).

The previous examples are especially favorable in that the functions chosen [(2), (9), and (14)] are com-

[3] This design is given, but not derived, by S. Muroga in "Elementary principle of parametron and its application to digital computers," *Datamation*, vol. 4, pp. 31–34; September/October, 1958.

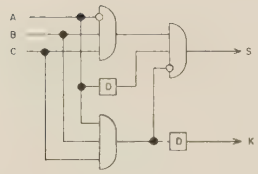

Fig. 3—Binary adder stage—majority-logic design.

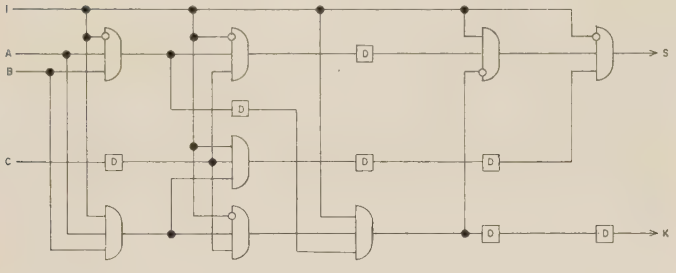

Fig. 4—Binary adder stage—conventional design.

pletely reducible to majority form. That is, each of these functions can be expressed exclusively in terms of "#" and NOT. Unfortunately, not all functions have this property. Even where it is not possible to replace all of the AND's and OR's by "#"s, however, application of the theorem may improve the design by replacing some of the AND's and OR's by "#"s. To illustrate this point, incompletely reducible functions are chosen as the two final examples.

The final $n=3$ example is

$$f(A_1, A_2, A_3) = A_1A_2 + A_1A_3 + \overline{A}_1\overline{A}_2A_3 = A_1(A_2 + A_3) + \overline{A}_1(\overline{A}_2A_3). \quad (16)$$

Comparison with (8) gives $X=A_1$, $f_1=A_2$, $f_2=A_3$, $f_3=\overline{A}_2$, and $f_4=A_3$. Application of (8) yields

$$f(A_1, A_2, A_3) = A_1 \# (A_1A_2 + \overline{A}_1\overline{A}_2) \# (A_1A_3 + \overline{A}_1A_3) \quad (17)$$

$$= A_1 \# (A_1A_2 + \overline{A}_1\overline{A}_2) \# A_3. \quad (18)$$

Application of (8) to the parenthesis of (18) yields

$$A_1A_2 + \overline{A}_1\overline{A}_2 = A_1(A_2 + 0) + \overline{A}_1(\overline{A}_2 \cdot 1) = A_1 \# (A_1A_2 + \overline{A}_1\overline{A}_2) \# (A_1 \cdot 0 + \overline{A}_1 \cdot 1) = A_1 \# (A_1A_2 + \overline{A}_1\overline{A}_2) \# \overline{A}_1. \quad (19)$$

Since the parenthesis of (19) is identical with that of (18), this function is shown to be irreducible. It is not, however, erroneous: that is,

$$A_1 \# (A_1A_2 + \overline{A}_1\overline{A}_2) \# \overline{A}_1 = A_1A_2 + \overline{A}_1\overline{A}_2. \quad (20)$$

The above example illustrates this important property of theorem (5): application of the theorem to any suitable function may either simplify the function or leave it unchanged. Conversion of (16) to (18), for example, simplifies (16), while conversion of the parenthesis of (18) to (20) leaves the parenthesis of (18) unchanged.

The final example of the interpretation and application of theorem (5) is the simplification of

$$f(A_1, A_2, A_3, A_4) = A_1A_2 + A_1A_3A_4 + A_2A_3, \quad (21)$$

which is an incompletely reducible $n=4$ case. The first step is to reduce (5) to the appropriate form for $n=4$ as follows:

$$X \sum_{i=1}^{3} f_i + \overline{X} \prod_{i=4}^{6} f_i = V_1 \# [V_1 \# V_2 \# V_3] \# V_4$$

$$X(f_1 + f_2 + f_3) + \overline{X}f_4f_5f_6 = m_4[X, (Xf_1 + \overline{X}f_4), (Xf_2 + \overline{X}f_5), (Xf_3 + \overline{X}f_6)] = X \# [X \# (Xf_1 + \overline{X}f_4) \# (Xf_2 + \overline{X}f_5)] \# (Xf_3 + \overline{X}f_6). \quad (22)$$

The reduction of (21) to the required form begins with the arbitrary decision that A_1 is X and proceeds as follows:

$$f(A_1, A_2, A_3, A_4) = A_1A_2 + A_1A_3A_4 + A_2A_3(A_1 + \overline{A}_1) = A_1A_2 + A_1A_3A_4 + A_1A_2A_3 + \overline{A}_1A_2A_3 = A_1A_2 + A_1A_3A_4 + \overline{A}_1A_2A_3 = A_1(A_2 + A_3A_4) + \overline{A}_1(A_2A_3). \quad (23)$$

Comparison of (22) and (23) gives $X=A_1$, $f_1=A_2$, $f_2=A_3A_4$, $f_3=0$, $f_4=A_2$, $f_5=A_3$, and $f_6=1$. Application of (22) to (23) yields

$$f(A_1, A_2, A_3, A_4) = A_1 \# [A_1 \# (A_1A_2 + \overline{A}_1A_2) \# (A_1A_3A_4 + \overline{A}_1A_3)] \# \overline{A}_1 = A_1 \# A_2 \# (A_1A_3A_4 + \overline{A}_1A_3). \quad (24)$$

The next step is to apply theorem (5) to the parenthesis of (24). Since only three independent literals (A_1, A_3, A_4) are included, it is convenient to rewrite as follows:

$$A_1A_3A_4 + \overline{A}_1A_3 \equiv B_1B_2B_3 + \overline{B}_1B_2. \quad (A_1 = B_1, A_3 = B_2, \text{and } A_4 = B_3.) \quad (25)$$

Application of (5) to (25) proceeds as follows:

$$f(B_1, B_2, B_3) = B_1B_2B_3 + \overline{B}_1B_2$$

$$X = \overline{B}_1, f_1 = B_2, f_2 = 0, f_3 = B_2, f_4 = B_3$$

$$f(B_1, B_2, B_3) = m_3[\overline{B}_1, (\overline{B}_1B_2 + B_1B_2), (\overline{B}_1 \cdot 0 + B_1B_3)] = \overline{B}_1 \# B_2 \# B_1B_3 = \overline{A}_1 \# A_3 \# A_1A_4. \quad (26)$$

The product A_1A_4 is irreducible, so substitution of (26) in (24) gives the final result.

$$f(A_1, A_2, A_3, A_4) = A_1 \# A_2 \# (\overline{A}_1 \# A_3 \# A_1A_4). \quad (27)$$

If $f(A_1,A_2,A_3,A_4)$ is implemented by three-input majority-decision elements, conventional design (with unconditional inputs) from (21) (factored) produces a network of five decision elements and six delays, whereas design from (27) produces a network of three decision elements and five delays. In this sense (27) is simpler than (21).

Limitations

The method introduced above does not apply with equal ease to all problems. Eqs. (3), (9), and (14), for example, are very susceptible to the method, while (16) and (21) are less so. The difficulties that prevent theorem (5) from providing an automatic method for reducing any given function to its simplest form are implicit in the examples and explicit in the paragraphs that follow.

In this context, the "simplest" form of a function is the one requiring the fewest decision elements or, if the number of decision elements is the same, the fewest delay elements. This simplest form ordinarily corresponds to the network that is the cheapest, lightest and smallest. It is usually also the fastest.

It is stated above that application of theorem (5) to any suitable function may simplify that function or leave it unchanged. Strictly speaking, however, the examples show that the immediate effect of applying (5) to a function is always to put that function into a more complicated form, which is then simplified by auxiliary identities hereafter referred to as *simplification lemmas*. Application of (5) to (16), for example, yields (17), which is more complicated than (16). The final reduction to (18) depends on tacit use of the simplification lemma

$$XY + X\overline{Y} \equiv X. \tag{28}$$

Similarly, the derivations of (15) and (20), respectively, use the following simplification lemmas:

$$\overline{X \# Y \# Z} \equiv \overline{X} \# \overline{Y} \# \overline{Z}, \tag{29}$$

and

$$X \# Y \# \overline{X} \equiv Y. \tag{30}$$

The examples illustrate the fact that theorem (5) is nearly useless unless supported by simplification lemmas. This fact would not constitute a problem if all of the required simplication lemmas were as simple as (28), (29), and (30). Unfortunately, however, many are not; their complexity and variety increase rapidly with increasing n.

Successful application of theorem (5) depends on judicious selection of X and of the f's (f_1, f_2, etc.). In the examples given above, selection of X is not difficult, and selection of the f's is almost automatic. Even for small n, however, there are cases in which these selections are not so easy (the optimum X is, in a few cases, a function of more than one of the literals in the given Boolean expression). The limitations on the usefulness of theorem (5) imposed by these difficulties are not serious for small n, but, unfortunately, they too increase rapidly with increasing n.

It is often possible to obtain the simplest form of any given function by applying theorem (5) repeatedly until further repetition produces no further simplification. This fact is illustrated by the derivation of (19) and the earlier examples. Because of the difficulties explained in the previous paragraphs, however, the simplest form can not, in general, be recognized with certainty. For example, even (27) can be further simplified to yield

$$f(A_1, A_2, A_3, A_4) = (A_1 \# A_2 \# A_3) \# A_3A_4 \# A_2,$$

which requires three decision elements and only one delay.

Proof

The first step in proving theorem (5) is to prove that

$$m_n(V_1, \cdots V_n) = V_1 \sum_{i=2}^{n} V_i + \overline{V}_1 \prod_{i=2}^{n} V_i. \tag{31}$$

Theorem (31) is proved inductively by demonstrating that 1) it is true for $n=3$, and 2) truth for $n=p$ entails truth for $n=p+1$ as well. Proof of 1) begins by combining (7) with the definition of "#" to obtain

$$\begin{aligned} m_3(V_1, V_2, V_3) &= V_1 \# V_2 \# V_3 \\ &= V_1V_2 + V_1V_3 + V_2V_3 \\ &= V_1V_2 + V_1V_3 + V_2V_3(V_1 + \overline{V}_1) \\ &= V_1V_2 + V_1V_3 + V_1V_2V_3 + \overline{V}_1V_2V_3 \\ &= V_1V_2 + V_1V_3 + \overline{V}_1V_2V_3 \\ &= V_1 \sum_{i=2}^{3} V_i + \overline{V}_1 \prod_{i=2}^{3} V_i. \end{aligned} \tag{32}$$

Proof of 2) begins with

$$m_p(V_1, \cdots, V_p) = V_1 \sum_{i=2}^{p} V_i + \overline{V}_i \prod_{i=2}^{p} V_i \tag{33}$$

being given and requires that

$$m_{p+1}(V_1, \cdots, V_{p+1}) = V_1 \sum_{i=2}^{p+1} V_i + \overline{V}_1 \prod_{i=2}^{p+1} V_i \tag{34}$$

be proved. Eq. (6) is applied to $n=p+1$ to give

$$\begin{aligned} m_{p+1}(V_1, \cdots, V_{p+1}) &= V_1 \# [m_p(V_1, \cdots, V_p)] \# V_{p+1} \\ &= V_1[m_p(V_1, \cdots, V_p)] + V_1V_{p+1} \\ &\quad + V_{p+1}[m_p(V_1, \cdots, V_p)]. \end{aligned}$$

Substitution from (33) gives

$$m_{p+1}(V_1, \cdots, V_{p+1}) = V_1 \sum_{i=2}^{p} V_i + V_1 V_{p+1} + V_1 V_{p+1} \sum_{i=2}^{p} V_i + \overline{V}_1 V_{p+1} \prod_{i=2}^{p} V_i$$

$$= V_i \sum_{i=2}^{p} V_i + V_1 V_{p+1} + \overline{V}_1 V_{p+1} \prod_{i=2}^{p} V_i$$

$$= V_1 \sum_{i=2}^{p+1} V_i + \overline{V}_1 \prod_{i=2}^{p+1} V_i,$$

which proves (34) and thereby completes proof of (31).

Comparison of (6) and (5) shows that

$$V_1 = X,$$
$$V_2 = (Xf_1 + \overline{X}f_n), \cdots, V_n = (Xf_{n-1} + \overline{X}f_{2n-2}). \quad (35)$$

Theorem (5) is proved by substituting (35) in (31) to obtain

$$\begin{aligned} m_n(V_1, \cdots, V_n) &= V_1(V_2 + V_3 + \cdots V_n) + \overline{V}_1 V_2 V_3 \cdots V_n \\ &= X[(Xf_1 + \overline{X}f_n) + (Xf_2 + \overline{X}f_{n+1}) + \cdots + (Xf_{n-1} + \overline{X}f_{2n-2})] \\ &\quad + \overline{X}(Xf_1 + \overline{X}f_n)(Xf_2 + \overline{X}f_{n+1}) \cdots (Xf_{n-1} + \overline{X}f_{2n-2}) \\ &= X(f_1 + f_2 + \cdots + f_{n-1}) + \overline{X}f_n f_{n+1} \cdots f_{2n-2} \\ &= X \sum_{i=1}^{n-1} f_i + \overline{X} \prod_{i=n}^{2n-2} f_i, \end{aligned}$$

which completes proof of (5).

The Use of Parenthesis-Free Notation for the Automatic Design of Switching Circuits*

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Summary—A parenthesis-free notation is introduced for the representation of series-parallel switching networks. The notation facilitates the calculation of circuit parameters and permits an unambiguous characterization of the circuit topology.

Given certain criteria for feasibility of a switching network related to the circuit parameter values, it is shown how an infeasible series-parallel network can be transformed into an equivalent feasible network by "cascading" operations applied to the two-terminal subnetworks of the original network. A systematic method is developed, resulting in an optimum choice of cascading operations such that the number of switching elements required to implement the transformed circuit is minimized relative to cascading.

I. Introduction

COMPUTERS are being used increasingly in the design and development of digital equipment. In particular, a number of techniques are available for the minimization of Boolean functions using computer programs [1]–[3]. Since Boolean addition and multiplication correspond respectively to parallel and series connections of switching elements, it is always possible to transform a Boolean equation into a corresponding series-parallel switching network.

Unfortunately, circuit theoretical considerations may restrict the direct implementation of minimized functions. It then becomes necessary to revise the original circuit configurations to satisfy circuit restrictions. In general, equivalent "feasible" configurations can be substituted for configurations that do not obey circuit rules; this is usually achieved at the cost of a number of additional circuit elements.[1]

In order to program a digital computer to make these substitutions, it is necessary to use a notation that unambiguously exhibits the structure of each configuration. Such a notation is the parenthesis-free notation first introduced by Lukasiewicz [4]. A parenthesis-free notation can be used effectively to represent series-parallel switching networks, to calculate certain dimensional parameters of the network, and to isolate all the two-terminal subnetworks.

For purposes of demonstration, direct coupled transistor logic will be used in some of the examples. In particular, unless otherwise specified, it is assumed that the circuits are implemented by transistor inverter

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[1] It might be more elegant conceptually to incorporate rules for the satisfaction of circuit constraints in the original process of circuit synthesis, instead of generating circuits which must later be modified if infeasible.

itches (inverters) connected either in series or in rallel. The notation and method are, however, laptable to other technologies.

II. Abstract Network Theory

A *two-terminal switching network* is defined abstractly a finite collection of two types of entities, *elements* $b, c, \cdots$ and *vertices* $1, 2, 3, \cdots$ with the following roperties:

1) With each element are associated two of the vertices, the combination forming a *branch*. A branch consisting of the element e and the vertices α and β will be symbolized by $e\ (\alpha, \beta)$.
2) The collection contains two special vertices called the *terminals* of the network. The two terminals will be labelled 1 and 2 respectively.

A *two-terminal subnetwork* of a network is a subnetork that has exactly two vertices in common with the emainder of the network. The two common vertices onstitute the terminals of the subnetwork.

A *path* is defined as a set of branches that can be rdered in the form $e_1(\alpha, \beta), e_2(\beta, \gamma), e_3(\gamma, \delta), \cdots, (\epsilon, \zeta)$; the path is said to *join* the vertices α and ζ. If one of the vertices $\beta, \gamma, \delta, \cdots, \epsilon$ appear in any other ranches of the network, the elements $e_1, e_2, \cdots, e_k$ re said to be connected in *series*. A *loop* is a set of ranches that can be ordered in the form $e_1(\alpha, \beta), e_2(\beta, \gamma), (\gamma, \delta), \cdots, e_k(\zeta, \alpha)$, the vertices $\alpha, \beta, \gamma, \cdots, \zeta$ being istinct as in the case of the path. A set of elements, very two of which (with their associated vertices) orm a loop, are said to be connected in *parallel*. A twoerminal switching network is *series-parallel*, if it is a eries or parallel combination of two series-parallel etworks; a single element is a two-terminal seriesarallel switching network [5].

To an abstract network as defined above, there corresponds a physical network. To each of the vertices , 2, 3, $\cdots$ there corresponds a connection point of the etwork, and to each of the elements $a, b, c, \cdots$ there orresponds a switch. The switches may be bilateral, in hich case $e(\alpha, \beta) = e(\beta, \alpha)$, or they may be unilateral, n which case a unique direction is assumed between he vertices α and β. A special element including a otential source in series with a current detector is often ssociated with the two terminals of the network.

Two abstract two-terminal series-parallel networks re shown in Fig. 1(a) and 1(b). It may be noted that ll series (parallel) connections in the network of Fig. (a) are replaced by parallel (series) connections reectively, in Fig. 1(b) and that the polarity of all witches is reversed. The networks are thus *duals* of ach other.

III. The Parenthesis-Free Notation

Consider a language composed of two types of characters: operators P_i and S_i of degree i, and variables

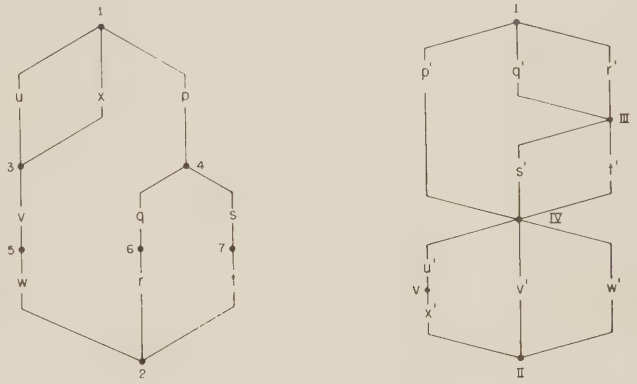


Fig. 1—Dual abstract two-terminal series-parallel networks.

$\{a, b, c, \cdots\}$. Let the two operators represent respectively a parallel and a series connection of i two-terminal subnetworks of a network, and let the lower case letters represent the variables assigned to the switches.[2] A two-terminal subnetwork can be a single branch or a more complicated array of several branches.

Since a series-parallel network is defined as a series or parallel connection of switching elements, the *P-S* language can clearly be used to represent any series-parallel switching network. For example, $P_3(x, y, z)$ represents a parallel connection of the three elements x, y, and z, while $P_2(S_2(a, b), c)$ represents the parallel connection of $S_2(a, b)$ and c, where $S_2(a, b)$ is itself a series connection of elements a and b.

A language whose words consist of operators of degree i, each followed by i operands, has been called a "simple" language [6]. It has been shown that for such languages the usual parentheses indicating grouping are redundant. Expressions can thus be written without parentheses or commas. Moreover, algorithms can be devised for transforming ordinary Boolean expressions into the corresponding parenthesis-free expressions, and vice versa [7].

As an example, the abstract two-terminal series-parallel network shown in Fig. 1(b) is implemented with transistor inverters as shown in Fig. 2. Terminal 1 is connected to a resistor leading to a potential source and to an output terminal f; terminal 2 is connected to ground. The network of Fig. 2 generates the function $f = p(qr + st) + (u + x)vw$.[3]

The parenthesis-free expression corresponding to the inverter array of Fig. 2 is given by

$$f = S_2P_2p'S_2P_2q'r'P_2s't'P_3S_2u'x'v'w'. \qquad (1)$$

[2] Thanks are given to a referee for pointing out that a similar notation was previously suggested by G. W. Patterson in the "Sixth Quarterly Progress Report on the Theory of Switching" of the Moore School of Electrical Engineering on the Theory of Switching (ASTIA No. AD 155-004, December, 1957).

[3] The configuration of Fig. 2, corresponding to that of Fig. 1(b), generates the function $f = p(qr + st) + (u + x)vw$, since direct-coupled transistor logic is used. If more familiar relay-like logic were used, the required configuration would be that of Fig. 1(a).

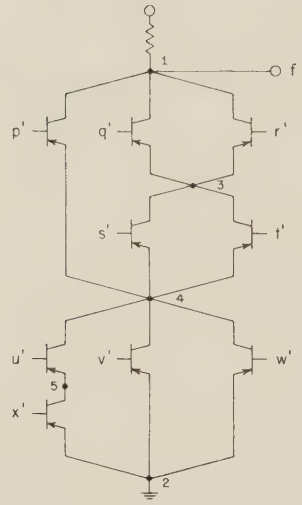


Fig. 2—Transistor inverter network for the function $p(qr+st)+(u+x)vw$.

A set of n adjacent characters starting with the left-most character in a parenthesis-free expression and proceeding to the right is called a *head* of length n. Similarly, the right-most n characters are defined as a *tail* of length n. In expression (1), $S_2P_2p'S_2$ is a head of length 4, and $u'x'v'w'$ is a tail of length 4.

A system of weights is assigned to the characters to distinguish legitimate parenthesis-free expressions from illegitimate ones and to aid in identifying the switching networks corresponding to specified expressions.[4] In particular, let the weight of the characters be specified as shown in Table I, and let the weight of an expression be the sum obtained by adding the character weights of all characters in the expression.

TABLE I
CHARACTER WEIGHTS

Character	Weight
Operators of degree i	$1-i$
Variables	1

A *well-formed formula* is then defined as an expression of weight $+1$ whose minimum tail weight is positive [8]. As an example, S_2xP_2yz is well-formed; S_2xyz has positive tail weight but is not well-formed since its total weight is $+2$; S_2xP_2y has a minimum tail weight of 0 and is thus not well-formed. It may be verified that the expression (1) is a well-formed formula.

A well-formed formula Δ is of the form

$$\Delta = [\delta, \Delta_{D(\delta)}, \cdots, \Delta_1]$$

[4] The unique identification of a series-parallel switching network corresponding to a given parenthesis-free expression depends on a convention associating the order in which various operators and variables are listed in the parenthesis-free expression, with the physical ordering of sub-networks within the two-terminal network. The uniqueness does not hold in the reverse direction, in that several distinct but equivalent parenthesis-free expressions can sometimes be found to represent a given switching network.

where δ is of length 1; $D(\delta)$ represents the degree of δ and each of the Δ_k is well formed. Given an operator δ it is possible to find subnetwork $\Delta_{D(\delta)}$ by summing the weights of the characters from *left to right* starting with the character immediately to the right of the operator δ, and continuing until the count reaches $+1$. Subnetwork $\Delta_{D(\delta)-1}$, associated with the same operator δ, is found similarly by resetting the count to zero, and summing the character weights from left to right starting with the first character to the right of the subnetwork $\Delta_{D(\delta)}$, and continuing until the new count reaches $+1$. The remaining subnetworks associated with δ are found by similar counting procedures. Each well-formed formula Δ_k is thus represented by a shortest head of positive weight.

The set obtained by taking the network associated with a given parenthesis-free expression, as well as the aggregate of all subnetworks associated with each of the operators in the expression, will be called the set of *constituent two-terminal subnetworks*. The constituent two-terminal subnetworks of expression (1) are isolated by the counting procedure shown in Table II.

Corresponding to each operator of degree $i>2$ occurring in a parenthesis-free expression, it is possible to

TABLE II
TWO-TERMINAL SUBNETWORKS FOR NETWORK OF FIG. 2

Operator	Sub-network Number	Subnetwork
—	1	$S_2\ P_2\ p'\ S_2\ P_2\ q'\ r'\ P_2\ s'\ t'\ P_3\ S_2\ u'\ x'\ v'\ u$ $-1-2-1-2-3-2-1-2-10-2-3-2-10+$
S_2	2	$P_2\ p'\ S_2\ P_2\ q'\ r'\ P_2\ s'\ t'$ $-1\ 0\ -1-2-1\ 0\ -1\ 0\ +1$
	3	$P_3\ S_2\ u'\ x'\ v'\ u$ $-2-3-2-10+$
P_2	4	p' $+1$
	5	$S_2\ P_2\ q'\ r'\ P_2\ s'\ t'$ $-1-2-10-10+1$
S_2	6	$P_2\ q'\ r'$ $-1\ 0+1$
	7	$P_2\ s'\ t'$ $-10+1$
P_2	8	q' $+1$
	9	r' $+1$
P_2	10	s' $+1$
	11	t' $+1$
P_3	12	$S_2\ u'\ x'$ $-10+1$
	13	v' $+1$
	14	w' $+1$
S_2	15	u' $+1$
	16	x' $+1$

fine *compound* two-terminal subnetworks by taking e constituent subnetworks corresponding to each erator, first two at a time, then three at a time, and, ally, $i-1$ at a time, and joining them by an operator appropriate degree. Consider, as an example, the P_3 erator and the three associated elementary subnetrks w', v', and $S_2u'x'$ of Table II. By taking the bnetworks two at a time and prefixing them by a P_2 erator, three additional compound two-terminal subtworks are obtained as follows:

⑰ $P_2\,S_2\,u'\,x'\,v'$,

⑱ $P_2\,S_2\,u'\,x'\,w'$,

⑲ $P_2\,v'\,w'$.

The total number of subnetworks that are isolated the weight counting procedure depends on the form the parenthesis-free expression being considered. In der to obtain *all* subnetworks of a given network, it necessary to operate upon a unique *reduced* form. The duced form of a parenthesis-free expression may be fined as that form which represents the corresponding ries-parallel network with a minimum number of perators. To obtain the reduced form, an attempt is ade to replace a set of P (S) operators by a single (S) operator of larger degree. Specifically, since a rallel (series) array of elements which are themselves parallel (series) with other elements is equivalent to a rger parallel (series) array, it is possible to use the llowing equivalences to reduce a parenthesis-free expression:

$$\left.\begin{aligned} P_i\,P_j\,x_1x_2\cdots x_{i+j-1} &= P_{i+j-1}\,x_1x_2\cdots x_{i+j-1}\\ S_i\,S_j\,x_1x_2\cdots x_{i+j-1} &= S_{i+j-1}\,x_1x_2\cdots x_{i+j-1}\end{aligned}\right\}. \quad (2)$$

n expression in reduced form has associated with it the aximum number of compound subnetworks, since ne degree of its operators is maximized.

Consider an expression δ, $\Delta_{D(\delta)}$, $\cdots$, Δ_1 where each f the Δ_k is well-formed and δ is an operator of degree (δ) as before. If the left-most character of any of the $_k$ is an operator of the same type as δ, that operator an be removed from the expression and $D(\delta)$ can be ncreased in accordance with the formulas (2). Each me a reduction is achieved, the subnetworks corresponding to the "incremented" operator are determined nd the process is repeated, until no further reductions re possible. When all operators in the expression have een treated and no further reductions are possible, the educed form is obtained.

The process is illustrated in Table III for the expression $P_3S_3aP_2bcS_2deP_3fS_2ghP_2iP_2jkl$. The operator eing operated upon is underlined and the corresponding subnetworks are shown by brackets. The elimination of an operator from one line of Table III to the ext is indicated by a circle.

All expressions shown in Table III correspond to the ame networks. The last expression represents the required reduced form.

TABLE III

Reduction Process for Parenthesis-Free Expressions

P_3	S_3	a	P_2	b	c	S_2	d	e	ⓟ$_3$	f	S_2	g	h	P_2	i	P_2	j	k	l
P_5	S_3	a	P_2	b	c	S_2	d	e		f	S_2	g	h	ⓟ$_2$	i	P_2	j	k	l
P_6	S_3	a	P_2	b	c	S_2	d	e		f	S_2	g	h		i	ⓟ$_2$	j	k	l
P_7	S_3	a	P_2	b	c	S_2	d	e		f	S_2	g	h		i		j	k	l
P_7	S_3	a	P_2	b	c	ⓢ$_2$	d	e		f	S_2	g	h		i		j	k	l
P_7	S_4	a	P_2	b	c		d	e		f	S_2	g	h		i		j	k	l

IV. Circuit Parameters

A number of important parameters characterize a series-parallel switching network. Among these,

E = number of elements in the circuit;
Q = number of paths, not including any loops, which join the two terminals of the network;
C = number of connection points, or vertices, of the network;
V = vertical dimension defined as the largest number of branches in any path which joins the two terminals and does not include a loop;
H = horizontal dimension defined as the vertical dimension of the dual network.

Because of the recursive definition of a series-parallel network, the parameter evaluation techniques are based on the fact that each parameter value for a complete network is a function of the parameter values of the constituent subnetworks. Thus, if the parameter values for the individual elements are known, the value for the complete expression can be determined recursively. In particular, given a series-parallel network, it is sufficient to know the value of each parameter for a single branch, for a parallel array of branches, and for a series array of branches. In the parenthesis-free expression this corresponds to the values for a single variable, for a set of well-formed formulas prefixed by a P operator, and for a set of well-formed formulas prefixed by an S operator. The recursive definition of the previously given parameters is shown in Table IV. In each case, X_k refers to the value of X for the kth constituent subnetwork operated upon by the P_i or S_i operator.

Consider, for example, the vertical and horizontal dimensions V and H. The values given reflect the fact that V and H are equal to 1 for a single element, and that a set of networks connected in series will have a vertical dimension equal to the sum of the vertical dimensions of the networks, and a horizontal dimension equal to the maximum of the horizontal dimensions of the networks. The values are reversed for networks connected in parallel.

All parameter values for a given network can now be calculated by a *single linear scan* from right to left through the characters of the corresponding parenthesis-

TABLE IV

RECURSIVE DEFINITION OF NETWORK PARAMETERS

Parameter	Single Element	Formula Prefixed by P_i Operator	Formula Prefixed by S_i Operator
E	1	$\sum_{k=1}^{i} E_k$	$\sum_{k=1}^{i} E_k$
Q	1	$\sum_{k=1}^{i} Q_k$	$\prod_{k=1}^{i} Q_k$
C	2	$\sum_{k=1}^{i} C_k - 2(i-1)$	$\sum_{k=1}^{i} C_k - (i-1)$
V	1	$\max_k V_k$ $k = 1, 2, \cdots, i$	$\sum_{k=1}^{i} V_k$
H	1	$\sum_{k=1}^{i} H_k$	$\max_k H_k$ $k = 1, 2, \cdots, i$

TABLE V

COMPUTATION OF VERTICAL DIMENSION FOR NETWORK OF FIG. 2

S_2	P_2	p'	S_2	P_2	q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	V
															w'	(1)
														v'	w'	(1)(1)
													x'	v'	w'	(1)(1)(1)
												u'	x'	v'	w'	(1)(1)(1)(1)
											S_2	u'	x'	v'	w'	(2)(1)(1)
										P_3	S_2	u'	x'	v'	w'	(2)
									t'	P_3	S_2	u'	x'	v'	w'	(1)(2)
								s'	t'	P_3	S_2	u'	x'	v'	w'	(1)(1)(2)
							P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(1)(2)
						r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(1)(1)(2)
					q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(1)(1)(1)(2)
				P_2	q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(1)(1)(2)
			S_2	P_2	q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(2)(2)
		p'	S_2	P_2	q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(1)(2)(2)
	P_2	p'	S_2	P_2	q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(2)(2)
S_2	P_2	p'	S_2	P_2	q'	r'	P_2	s'	t'	P_3	S_2	u'	x'	v'	w'	(4)

free expression. For each character in the expression, a parameter value is computed in accordance with the formulas of Table IV. When the left-most character is treated, the correct parameter value for the complete network will have been obtained.

As an example, the complete computation for the vertical dimension V of the network of Fig. 2 is detailed in Table V. Each time a variable is scanned, a (1) is added to the accumulated string of dimensions of constituent subnetworks. Each time a P_i or S_i operator is scanned, the i dimensions of its constituents are removed from the string, and their sum or maximum is substituted in accordance with the formulas of Table IV. The vertical dimension computed when the left-most operator is scanned is 4. It may be seen from Fig. 2 that this is indeed the correct dimension of the network. This value corresponds to one of the paths including the connection points 1, 3, 4, 5, and 2. The other parameter values may be similarly ascertained. For the network of Fig. 2 corresponding to expression (1), one obtains respectively $E=9$, $Q=15$, $C=5$, and $H=3$.

Depending upon the switching elements used, certain additional parameters may be related to the feasibility of a network. For example, if transistor inverters are connected in series and parallel, the number of distinct, simultaneously conducting transistors that lie between any given transistor and the output terminal is a limiting factor. Accordingly, the *collector loading of a switching element* may be defined abstractly as the number of distinct elements that lie on all paths, excluding loops, between the given transistor and the output terminal. In Fig. 2 the collector loading of the s' transistor is 2, since the transistors q' and r' lie between the s' transistor and the output terminal. The *collector loading of a network* may be defined as the maximum of the collector loadings of its elements. Thus, the collector loading of the network in Fig. 2 is 6 corresponding to the loading of the x' transistor.[5]

It is apparent that the collector loading of a network is affected by the ordering of its constituent subnetworks. Consider a series connection of i subnetworks. The collector loading of the complete network is

$$L = \sum_{k=1}^{i} E_k + L_j, \qquad k \neq j \tag{3}$$

where L_j is the collector loading of the constituent subnetwork located closest to terminal 2, *i.e.*, closest to ground. Eq. (3) is minimized to give

$$L_{\min} = \sum_{k=1}^{i} E_k + \min_k \{L_k - E_k\}. \tag{4}$$

Thus, for a set of subnetworks connected in series, that subnetwork should be placed closest to ground for which $L_k - E_k$ is smallest. If a set of subnetworks is connected in parallel, the collector loading of the complete network is simply the maximum collector loading of the subnetworks.

As before, the collector loading of a given network can be computed recursively in terms of the collector loadings of the constituent subnetworks. The relevant formulas are shown in Table VI, where L is taken to be the minimum value of the collector loading over any reordering of constituent subnetworks, and L' is the collector loading for the dual network. The formulas for the element count E are repeated from Table IV for completeness.

To compute the collector loading, the characters in the parenthesis-free expression are again scanned one at

[5] The definition of the collector loading given above for an abstract network is somewhat more restrictive than the actual restriction on the corresponding physical network. Loading is actually determined only by those elements which may be simultaneously in a conducting state.

time from right to left. It is necessary, however, to ore for each elementary subnetwork a pair of digits , E) corresponding to the collector loading and the ement count. Each time a variable is treated, the pair , 1) is added to the string; for P_i and S_i operators, the ordered pairs corresponding to the i constituent sub-tworks are used to compute a new ordered pair in cordance with the formulas of Table VI. The compu-tion of the collector loading for the network of Fig. 2 shown in Table VII. It may be seen that the collector ading is found to be equal to 6 and the transistor unt equal to 9.

TABLE VI

RECURSIVE DEFINITION OF COLLECTOR LOADING

Parameter	Single Element	Formula Prefixed by P_i Operator	Formula Prefixed by S_i Operator
E	1	$\sum_{k=1}^{i} E_k$	$\sum_{k=1}^{i} E_k$
L	0	$\max_k L_k$ $k = 1, 2, \cdots, i$	$E + \min_k \{L_k - E_k\}$
L'	0	$E + \min_k \{L_k' - E_k\}$	$\max_k L_k'$ $k = 1, 2, \cdots, i$

TABLE VII

COMPUTATION OF COLLECTOR LOADING FOR NETWORK OF FIG. 2

S_2 P_2 p' S_2 P_2 q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(L, E)
w'	(0, 1)
v' w'	(0, 1)(0, 1)
x' v' w'	(0, 1)(0, 1)(0, 1)
u' x' v' w'	(0, 1)(0, 1)(0, 1)(0, 1)
S_2 u' x' v' w'	(1, 2)(0, 1)(0, 1)
P_3 S_2 u' x' v' w'	(1, 4)
t' P_3 S_2 u' x' v' w'	(0, 1)(1, 4)
s' t' P_3 S_2 u' x' v' w'	(0, 1)(0, 1)(1, 4)
P_2 s' t' P_3 S_2 u' x' v' w'	(0, 2)(1, 4)
r' P_2 s' t' P_3 S_2 u' x' v' w'	(0, 1)(0, 2)(1, 4)
q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(0, 1)(0, 1)(0, 2)(1, 4)
P_2 q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(0, 2)(0, 2)(1, 4)
S_2 P_2 q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(2, 4)(1, 4)
p' S_2 P_2 q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(0, 1)(2, 4)(1, 4)
P_2 p' S_2 P_2 q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(2, 5)(1, 4)
S_2 P_2 p' S_2 P_2 q' r' P_2 s' t' P_3 S_2 u' x' v' w'	(6, 9)

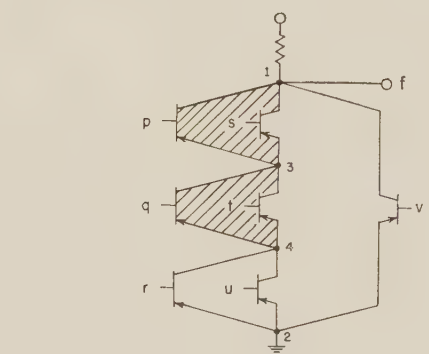
V. CIRCUIT RESTRICTIONS

The parameters defined in the preceding section are elated to actual restrictions on series-parallel switching ircuits. For example, for transistor circuits, the values f H, L, and V must generally not exceed certain ritical values H_0, L_0, and V_0. Restrictions of this type nay be classified as *dimensional restrictions*.

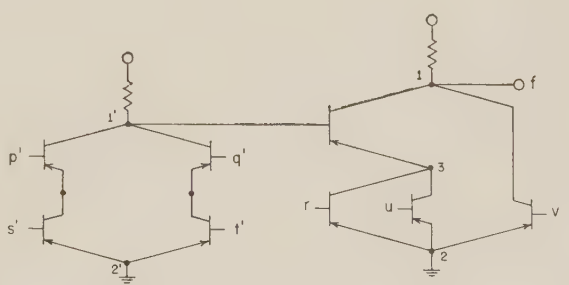
Another type of restriction is imposed by the un-vailability of certain input polarities. If input signal x s available, but not x', the circuitry must be designed o use only x. Restrictions of this type may be classified s *polarity restrictions*.

Both types of restrictions can be satisfied by using he *cascading operation*. The cascading operation is ased on the fact that the output of a switching circuit s unaffected if any two-terminal subnetwork is re-noved, and a functionally equivalent network is sub-tituted. In the case of a transistor inverter network, ny subnetwork can be replaced by a single transistor, nd the dual of the subnetwork cascaded into this ransistor. Such a substitution is illustrated in Fig. 3.

To dualize a cascaded subnetwork, it is sufficient to lter the corresponding parenthesis-free expression by eplacing P by S, S by P, and primed (unprimed) vari-



(a)



(b)

Fig. 3—(a) Transistor inverter network prior to cascading. (b) Equivalent network resulting from cascading operation.

ables by unprimed (primed) ones. The cascading operation itself can be indicated by prefixing the expression of the dualized submatrix with a C_1 operator. The cascade operator stands for the transistor which replaces the dualized subnetwork in the original network. Consider, for example, the network of Fig. 3. The expression for the subnetwork being cascaded is $S_2\ P_2\ p\ s\ P_2\ q\ t$; the dualized input to the cascade operator C_1 will then be $P_2\ S_2\ p'\ s'\ S_2\ q'\ t'$ and the expression for the complete array of Fig. 3(b) is $P_2\ S_2\ C_1\ \{P_2 S_2 p' s' S_2 q' t'\} P_2\ r\ u\ v$.

The cascading operation can be defined similarly for non-inverting switches, such as transistor emitter followers. However, whereas for an inverter network a two-terminal subnetwork must be replaced by a single element whose input is the dual of the function generated by the subnetwork, no dualization is required for emitter followers.

A circuit resulting from the repeated application of cascading operations is a tree-like structure of cascaded subnetworks, as shown schematically in Fig. 4. Each cascading operation generates a new network and increases the cost of the complete circuit by one additional circuit element.

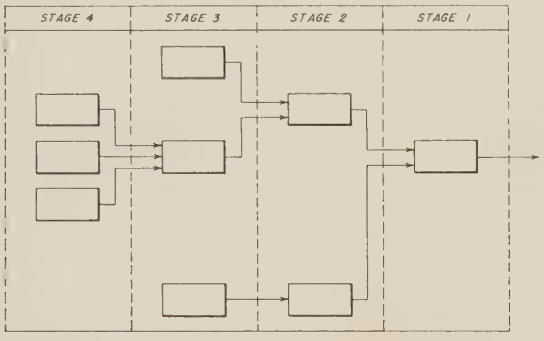


Fig. 4—Circuit resulting from repeated application of cascading operations.

Since each dimensional parameter of a network is a monotonically nondecreasing function of the parameter values of the constituent subnetworks, cascading operations tend to decrease the parameter value for the entire network, by substituting single switching elements for larger constituents. As an example, the network of Fig. 3(a) has dimensional parameter values equal to $V=3$, $H=3$, and $L=4$. The same parameters are equal to $V=2$, $H=3$, and $L=1$ for the two-terminal subnetwork on the right-hand side of Fig. 3(b), and to $V=2$, $H=2$, and $L=2$ for the cascaded subnetwork on the left-hand side of Fig. 3(b).

The cascading operation is also useful in satisfying polarity restrictions. If an inverter network contains a transistor whose input, x, is not available, then some subnetwork containing x can be cascaded, and the available polarity x' can be used to form the dual.

While it is always possible to find a combination of cascading operations to transform an infeasible network into one satisfying the dimensional restrictions, each cascaded subnetwork may have to be transformed in turn by further cascading operations. In fact, several physical stages may have to be created before a satisfactory circuit is obtained. Each cascading operation places the cascaded subnetwork one stage further from the output of the complete circuit. A limit for the number of stages is set by *delay restrictions*.

A nominal delay D can be assigned to the output of a circuit if the delay associated with each input is known. If D_i is the delay relative to a clock pulse, associated with the ith input of the circuit, and s_i is the stage at which the input enters (counting the stage closest to the final output as 1, the next stage as 2, etc., as shown in Fig. 4), then the delay D associated with the output of the circuit is

$$D = \max_i (D_i + s_i\tau),$$

where τ is the nominal delay assigned to each cascaded network. Clearly, the delay is lessened if the more-delayed inputs are entered at the stages closest to the output of the total circuit.

If the delay of the final output of a circuit is to be less than some critical value D_0, the delay associated with a network cascaded into the jth stage must be no more than $D_j = D_0 - j\tau$. Similarly, the variable x may be an input to a network at the jth stage if and only if $D_x \leq D_0 - j\tau = D_j$.

A *feasible two-terminal network* can now be defined as one whose dimensional parameters do not exceed certain critical values, whose inputs are available in the required polarities, and whose output is delayed by no more than some critical value, depending upon the stage at which the network is located in a larger circuit. A *feasible circuit* is either a feasible two-terminal network, or a set of cascaded networks, each of which is feasible. Since the output of each cascaded network leads to only one other network, output loading is not a factor in determining feasibility.

The problem of generating feasible circuits by cascading operations in the most efficient way can now be formulated as follows, given

1) a single network N,
2) a set of critical values for the height, width, and possibly collector loading,
3) a list of unavailable polarities for all input variables,
4) delay values D_0 and τ, and the delays associated with each polarity of each input,

to transform the network N into a feasible circuit using a minimum number of cascading operations.

VI. The Minimization Procedure, Exclusive of Delay Restrictions

It is evident that by generating all possible combinations of cascading operations, the feasible circuit or circuits with the fewest cascading operations may be exhaustively determined. A systematic procedure will now be described for obtaining the same result in a non-exhaustive fashion. Specifically, given an expression in parenthesis-free notation corresponding to a switching network, the set of all subnetworks of the complete network is generated by the reduction and weight-counting procedure described in Section III. Each of these subnetworks is then examined for feasibility using the parameter calculation techniques described in Section IV. The set of feasible subnetworks thus found is used to determine feasible circuits for those subnetworks that can be rendered feasible with a single cascading operation. Feasible circuits generated by two, three, $\cdots$, n cascading operations are successively determined until a feasible circuit is generated for the entire network. This is done by using at each step feasible circuits formed by 0, 1, 2, $\cdots$, i cascading operations to find feasible circuits with $i+1$ cascading operations.

The procedure will now be formalized. Let the *order* of a network be defined as the least number of cascading operations required to transform the network into a feasible circuit. In the present development, delay is not assumed to be a factor affecting the feasibility of a network. Let the sets R_0, R_1, R_2, $\cdots$, R_{i-1} contain all subnetworks of a given network that are of order 0, 1, 2, $\cdots$, $i-1$. Similarly, let the sets R_0', R_1', $\cdots$, R_{i-1}' contain the corresponding subnetworks for the dual of the given network. If inverter elements are used as circuit elements the sets R_0, R_1, $\cdots$, R_{i-1} can be used to determine all the members of R_i'. Similarly, the sets R_0', R_1', $\cdots$, R_{i-1}' can be used to determine all the members of R_i.[6]

Specifically, the set R_i is formed by considering all the subnetworks that are not members of R_0, R_1, $\cdots$, R_{i-1}. For each of those subnetworks, an attempt is made to demonstrate that i cascading operations will transform it into a feasible circuit. In the case of an inverter array, this can be done by finding some subnetwork whose dual is of order $i-1$, such that when the subnetwork is cascaded, the given network is rendered feasible. Alternatively, it can be done by taking i subnetworks, whose duals are feasible, such that when all the subnetworks are cascaded, the given network is rendered feasible. More generally, it is necessary to find sets of j subnetworks such that

$$\sum_{k=1}^{j} r_k + j = i,$$

where r_k is the order of the dual of the kth subnetwork. To ascertain that a given set of j cascading operations render the given network feasible, it is possible to substitute a single element for each cascaded subnetwork in the parenthesis-free expression, to recalculate the dimensional parameters as previously described, and to verify that the required polarities for all input variables are available.

Consider a given set of j subnetworks from the sets R_0', R_1', $\cdots$, R_{i-1}' which may be cascaded to render a given network feasible. A particular subnetwork is either included in the given combination of j subnetworks, or it is not included. If a particular subnetwork is included, then no other subnetwork is included that has circuit elements in common with it, since it is not possible to cascade overlapping subnetworks. If a particular subnetwork is not included, it may be necessary to include others, in order to render the network feasible; hence not all possible combinations of subnetworks need be considered.

A convenient, graphical means for examining the logical alternatives is to lay out the problem as a tree composed of nodes and arcs [2], [9]. Each node corresponds to a set of cascaded subnetworks, and each arc stands for the inclusion into the cascaded set or exclusion from the cascaded set of a given subnetwork.[7]

The significant information associated with each node is

1) a set A of j subnetworks that have been included in the combination of cascading operations,
2) a set B of subnetworks that have yet to be either included or excluded,
3) the cost $\sum r_\kappa + j$ associated with the cascading operations already included in set A.

Two arcs may extend from a given node. One arc, called the I-arc, leads to a node, at which a subnetwork contained in set B has been *included* in the combination of cascading operations. The other arc, called the E-arc, leads to a node at which the *same* subnetwork has been *excluded*.

No arcs lead from a node that has been *terminated*. A node is terminated if

1) no combination of cascading operations drawn from the subnetworks that remain in B would be sufficient to render the given network feasible, at any cost;
2) the cost associated with the node is i or greater, where i is the cost of the feasible circuit to be generated.

It is evident that if a suitable combination of subnetworks exists, it will be associated with one of the terminal nodes of the tree.

[6] If circuit elements are used that do not require dualization of the cascaded subnetworks, R_0, R_1, $\cdots$, R_{i-1} could be used directly to determine R_i.

[7] In the actual computer procedure, the tree can be replaced by a listing of subnetworks with a defined lexicographic ordering.

The branching procedure for finding a circuit of cost i for a given network may be outlined as follows. At the initial node of the tree, the set A is empty; the cost is zero; and the set B consists of all the subnetworks of the given network that are members of R_0', R_1', $\cdots$, or R_{i-1}'. In actual practice, many of these sets may be empty and thus contain no subnetworks. The number of branching operations may be lessened if the subnetworks in B are ordered by number of included elements. Each branching operation is then performed with respect to that subnetwork of set B which includes the largest number of circuit elements. The information associated with the node terminating an E-arc is the same as the information associated with the previous node, except that one member of B has been eliminated. The I-node, on the other hand, is created by transferring the included member to A, augmenting the cost, and eliminating from B those members that have elements in common with the included subnetwork.

Before a new branch is created at a node, a *sufficiency test* is performed to determine if the set B is sufficient to render the given network feasible, at any cost. If the sufficiency test fails, it is fruitless to continue branching from the node in question.

A simple test of sufficiency consists in attempting to cascade in turn all of the subnetworks remaining in set B. If two or more subnetworks have an element in common, a single cascading operation is performed for the combination. The resulting network is examined for feasibility and if it is infeasible the sufficiency test fails.

As an example of the complete branching procedure, consider the expression

$$S_2\ P_2\ S_2\ t\ u\ x\ P_3\ v\ w\ S_2\ y\ z. \tag{5}$$

Let the dimensions V, H, and L be restricted to $V \leq 3$, $H \leq 2$, and $L \leq 2$ and let inputs u and y be available only in the positive polarity and inputs x and v only in the negative polarity. A computation of the dimensions indicates $V=4$, $H=3$, and $L=4$. The complete network is thus not of order 0 and one or more cascading operations are necessary to render the network feasible.

The network has 14 subnetworks (excluding the complete network). The duals of six of these subnetworks are feasible; these six dualized subnetworks thus constitute the set R_0'. The duals of the remaining eight subnetworks are feasible at the cost of one additional circuit element; they thus constitute R_1'. The fourteen subnetworks and their feasible duals are shown in Table VIII.

It may be ascertained that the cascading of any member of R_0' is not sufficient to render the complete network feasible. The complete network is thus not of order 1. For purposes of illustration, the computations are thus started using the subnetworks of Table VIII.

At the origin of the tree, the cost is zero and the set

TABLE VIII

SUBNETWORKS AVAILABLE FOR CASCADING FOR NETWORK OF FIG. 6(a)

	Subnetworks		Feasible Duals
①	t	R_0'	t'
②	v		v'
③	w		w'
④	x		x'
⑤	z		z'
⑥	$P_2\ v\ w$		$S_2\ v'\ w'$
⑦	u	R_1'	$C_1\ u$
⑧	y		$C_1\ y$
⑨	$S_2\ t\ u$		$P_2\{C_1\ u\}t'$
⑩	$S_2\ y\ z$		$P_2\{C_1\ y\}z'$
⑪	$P_2\ S_2\ t\ u\ x$		$S_2\{C_1\ S_2\ t\ u\}x'$
⑫	$P_2\ v\ S_2\ y\ z$		$S_2\ v'\{C_1\ S_2\ y\ z\}$
⑬	$P_2\ w\ S_2\ y\ z$		$S_2\ w'\{C_1\ S_2\ y\ z\}$
⑭	$P_3\ v\ w\ S_2\ y\ z$		$S_2\ v'\{C_1\ P_2\ w\ S_2\ y\ z\}$

of networks available for cascading is numbered 1–14. An attempt is first made to cascade subnetwork 14. At node E14 (exclude 14), the cost is still zero and the subnetworks still available are 1–13. At node I14 (include 14) on the other hand, the cost is 2 since the dual of subnetwork 14 is of order 1 and one additional circuit element is required to cascade the subnetwork. Furthermore, only subnetworks 1, 4, 7, 9, and 11 are still available for cascading, since any subnetwork including elements v, w, y, or z must be eliminated. The expression for the complete network at node I14 becomes

$$S_2\ P_2\ S_2\ t\ u\ x\{C_1\ S_2\ v'[C_1\ P_2\ w\ S_2\ y\ z]\}. \tag{6}$$

It may be verified that the complete network is still infeasible since input x is unavailable in the positive polarity. At least one additional subnetwork including element x must thus be cascaded to render the network feasible.

The branching operations are illustrated by the tree of Fig. 5. Next to each node are shown the cost, the I-(included) subnetworks, the E-(excluded) subnetworks, and the set of subnetworks still available for cascading (in square brackets). The network obtained at node I14 I4 is feasible at a cost of 3. The corresponding expression is

$$S_2\ P_2\ S_2\ t\ u\{C_1\ x'\}\{C_1\ S_2\ v'[C_1\ P_2\ w\ S_2\ y\ z]\}. \tag{7}$$

It may be noted that while the complete network is of order 3, the duals of all subnetworks of the network are of order 0 or 1. Sets R_2', R_3', $\cdots$, are therefore empty and need not be considered in the branching process for the example. All the open nodes of the tree which have a

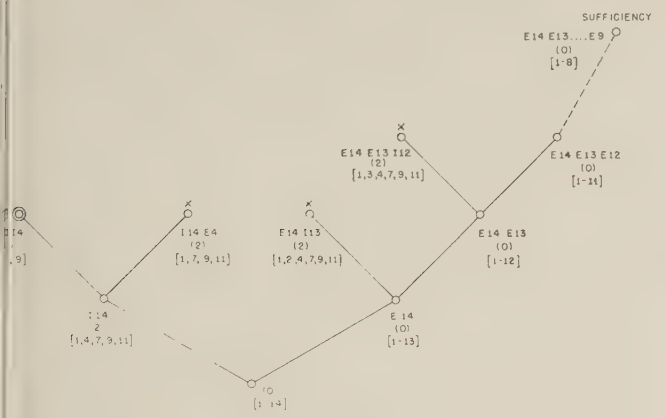


Fig. 5—Branching procedure for subnetworks of Table VIII.

ost of 2 and do not correspond to a feasible solution an be terminated, since they cannot possibly yield a easible solution at a cost of less than 3. This is indicated by an X above the corresponding node in Fig. 5. ode E14 E13 E12 E11 E10 E9 can be terminated because of failure of the sufficiency test.

The original infeasible network, as well as the infeasible network at node I14 and the final feasible network at node I14 I4 are illustrated in Fig. 6(a)–6(c), respectively. The networks of Fig. 6(b) and 6(c) require respectively two and three more circuit elements than he original network of Fig. 6(a).

VII. The Minimization Procedure, Including Delay Restrictions

Delay considerations may restrict some inputs to certain physical stages. For example, input x may be available at stages 1, 2, and 3, and not at stages 4, 5, 6, $\cdots$, and x' may be available at stages 1, 2, 3, and 4, and not at stages 5, 6, 7, $\cdots$. Such restrictions may prevent a given subnetwork from being cascaded at stage $j+1$, although it may be cascaded at stage j. In general, it is seen that the number of possible cascading operations becomes smaller at stages further from the output of the circuit. Because possible cascading operations are more restricted, it may become more costly to render a given subnetwork feasible at these stages.

It is convenient to designate the order of a network at each stage. In particular, one may define the set $R_i(j)$ as the set of networks which, when located at stage j, require a minimum of i cascading operations to transform them into feasible circuits.

Again assuming transistor inverters as circuit elements, the sets $R_0(j)$, $R_1(j)$, $\cdots$, $R_{i-1}(j)$ can be used to determine all the members of $R_i'(j-1)$. Conversely, the sets $R_0'(j)$, $R_1'(j)$, $\cdots$, $R_{i-1}'(j)$ can be used to determine all members of $R_i(j-1)$.

Since every feasible network of cost i at stage $j-1$ results from a cascading of subnetworks drawn from the sets $R_0(j)$, $R_1(j)$, $\cdots$, $R_{i-1}(j)$ or $R_0'(j)$, $R_1'(j)$, $\cdots$,

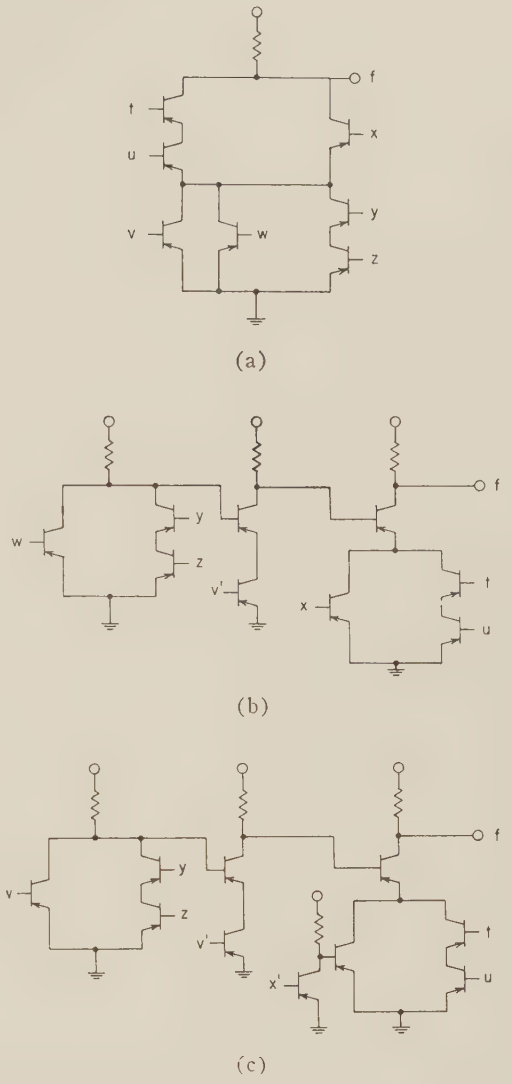


Fig. 6—(a) Infeasible network corresponding to expression (5) before cascading. (b) Infeasible network corresponding to expression (6). (c) Feasible network corresponding to expression (7).

$R_{i-1}'(j)$, the members of these sets constitute the set B. The branching procedure is then identical to that previously described. The sequence in which the various sets are determined is as follows:

1) $R_0(1)$
2) $R_0'(2)$
3) $R_1(1)$
4) $R_0(3)$
5) $R_1'(2)$
6) $R_2(1)$, etc.

This sequence may be represented graphically, as shown in Fig. 7. The figure is swept diagonally, starting with the set $R_0(1)$ in the upper left-hand corner, then going to the sets on the next diagonal, $R_0'(2)$, $R_1(1)$ and so on.

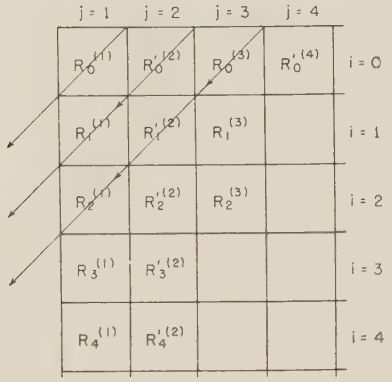


Fig. 7—Sequence of generation of sets $R_i(j)$.

The procedure is continued until the original network is found to belong to some set $R_i(1)$, or until it is evident that no feasible circuit will be found at any finite cost i. A sufficient condition for terminating the procedure is for stage 1 to be *complete*. Stage j is said to be complete if:

1) feasible circuits have been found for all subnetworks whose inputs are permitted to enter at stage j in one polarity or the other,

or

2) if feasible circuits have not been found for all these subnetworks, stage $j+1$ is complete, and each node of the tree for each remaining subnetwork is terminated because of failure of the sufficiency test.

If there are no delay restrictions, a solution will in general be found since the number of stages is then unlimited, and subnetworks can be cascaded at will. If delay restrictions exist, a solution may or may not be possible.

The method described offers a systematic, mechanized means for obtaining a feasible circuit, subject to restrictions of dimension, polarity, and delay. Although the circuit that is obtained is not necessarily the most economical implementation of an arbitrary Boolean function, it is the most economical circuit that can be obtained from a given network by cascading operations.

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DC Amplifier Misalignment in Computing Systems*

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Summary—The equivalent input circuit representation for dc misalignment (offset) has appeared in the literature for the special case of a vacuum tube voltage amplifier with infinite input impedance. This paper will generalize the concept of the equivalent input circuit representation for dc offset for the four amplifier types with finite input impedances, and will give the conditions under which the use of each equivalent circuit is justified. In each case, two offset generators which are characteristic of the amplifier alone—independent of driving source impedance and load impedance termination—are defined. Because of this independence, the offset generators are referred to herein as "characteristic misalignment generators." When the amplifier is connected into a system, a knowledge of these generators permits calculation of the effect of amplifier offset on system performance.

Treated in some detail is the finite input impedance voltage amplifier case. It is shown how the characteristic generators are evaluated in general for this case, and how these generators may be used in determining the effects of amplifier offset in computing systems employing dc operational amplifiers. In addition, the characteristic generators are derived for a transistorized dc-voltage-type amplifier containing a grounded emitter input stage.

By analogy it is seen that "characteristic noise generators," similar to the characteristic misalignment generators, may completely represent the internal noise of an amplifier.

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I. Introduction

REFERENCE in the literature to the equivalent input circuit representation for dc misalignment (offset) seems to have been specialized to the vacuum tube, infinite input impedance voltage ampli-

ier case.[1–3] Cases involving other amplifier types such s current amplifiers, transfer admittance amplifiers, as ell as amplifiers with finite input impedance, appar- ntly have not been treated. Just what form each quivalent input circuit should take, if one exists at all, nd the conditions under which its use is justified, has ot been shown to this writer's knowledge. With the dvent of the low input impedance transistorized mplifier, the need for a more generalized treatment ecomes emphasized. This treatment is to be considered erein.

In a previous report,[4] the *existence* of an equivalent input circuit representation for dc misalignment (or "offset") has been shown, and its use justified (subject o certain approximations) for each of the four possible ypes of dc amplifiers with finite input impedance. As might be surmised, the circuits are similar in form to hat for the known case (infinite input impedance voltage amplifier case). The four amplifier types considered were: 1) voltage, 2) current, 3) transfer admittance, and 4) transfer impedance. The equivalent input and output circuit representations for these amplifier types were shown to be as in Figs. 1, 2, 3, and 4, respectively (p. 354). In each figure the actual amplifier is replaced by an ideal amplifier having the same open or short circuit transfer characteristic but having infinite or zero input and output impedances, depending upon the amplifier type. The input and output impedances of the actual amplifier are simulated in the equivalent circuit by showing these quantities external to the ideal amplifier.

Also shown in the input circuit of each of these figures are the equivalent input misalignment voltage and current generators E_M and I_M. E_M and I_M are termed the "characteristic misalignment generators" because, subject to certain reasonable approximations, these generators are unaffected by: 1) the impedance of the source driving the input of the amplifier and 2) the load impedance connected to the output of the amplifier. That is, these generators "belong" to the amplifier alone, independent of driving source and load impedance terminations and, hence, completely characterize the amplifier with regard to its internal misalignment sources. It should not be construed, however, that each of the E_M and I_M quantities for a particular amplifier type (of the four types) has the same value as the corresponding quantity for any of the other types. Each E_M and I_M value is, in general, evaluated in a different manner depending upon the amplifier type.

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The assumptions employed in deriving and justifying the existence and use of the equivalent input circuits are these:

1) The amplifier input impedance is essentially independent of the load impedance connected to the output terminals of the amplifier.
2) The amplifier output impedance is essentially independent of the driving source impedance connected to the input terminals of the amplifier.
3) The significant internal misalignments, wherever they occur within the amplifier, are essentially unaffected by load impedance variations.

The above assumptions are valid for most (if not all) well designed computing type dc amplifiers. Assumptions 1) and 2) above imply that the amplifier input and output circuits are essentially isolated from each other; this is the usual case even for transistorized amplifiers. Since the major sources of misalignment occur usually within the first two stages (*i.e.*, the input stages) of the amplifiers, assuming each of these stages has significant gain (15 to 20 db), it follows that the output of the second stage of the amplifier must have sufficient isolation from load variations occurring at the output of the last stage for assumption 3) to be valid. The latter is usually the case.

In this paper we will show how these characteristic generators are evaluated in general, and how the equivalent input circuit containing these generators may be employed in analog computing systems for determining the effects of misalignment in dc operational amplifiers on system performance. In addition, we shall derive the characteristic generators for a transistorized dc amplifier having a grounded emitter type of input stage (assuming misalignments caused by succeeding stages are insignificant). It should be understood that the term "characteristic misalignment generator," which is used throughout this paper, is synonymous with the term "offset generator," which is widely used in the computer field.

II. Evaluation of the Characteristic Misalignment Generators

The characteristic misalignment generators will be evaluated for the finite input impedance voltage amplifier case—the case finding wide application in analog computing systems. Similar evaluations may be deduced for the other amplifier types.

Consider a voltage amplifier as in Fig. 1. Various sources of internal misalignment (M) may be present. Typical sources are:

1) Changes in component values due to environment (such as temperature) and aging.
2) Power supply potential changes.
3) Changes in leakage resistance paths from high potential sources to circuit nodes.

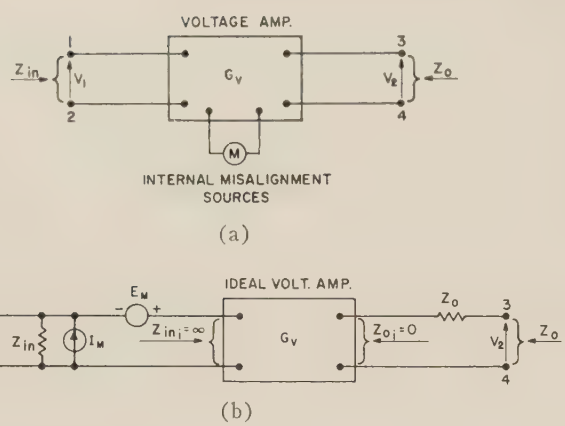


Fig. 1—Voltage amplifier. (a) Actual voltage amplifier. (b) Equivalent circuit representation for (a), showing characteristic misalignment generators E_M and I_M.

G_v = open circuit voltage transfer ratio
$G_v = V_2/V_1$ with $M=0$, Z_L (Load) $= \infty$
Z_{in} = input impedance
Z_o = output impedance
$Z_{in_i} =$ input impedance of ideal amplifier $= \infty$
$Z_{o_i} =$ output impedance of ideal amplifier $= 0$
E_M = equivalent input misalignment voltage generator
I_M = equivalent input misalignment current generator.

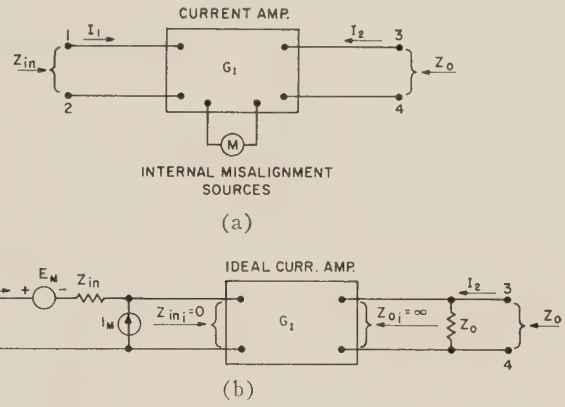


Fig. 2—Current amplifier. (a) Actual current amplifier. (b) Equivalent circuit representation for (a), showing characteristic misalignment generators E_M and I_M.

G_I = short circuit current transfer ratio
$G_I = -I_2/I_1$ with $M=0$, Z_L (Load) $= 0$
$Z_{in_i} =$ input impedance of ideal amplifier $= 0$
$Z_{o_i} =$ output impedance of ideal amplifier $= \infty$
E_M = equivalent input misalignment voltage generator
I_M = equivalent input misalignment current generator.

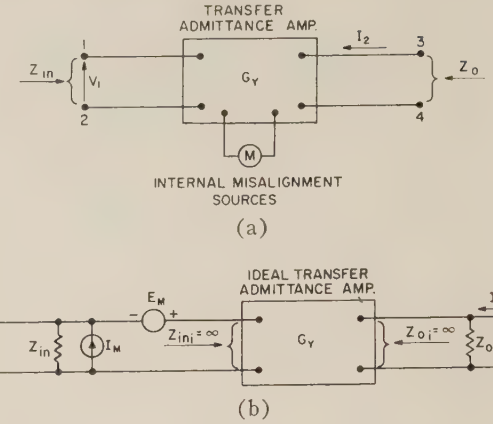


Fig. 3—Transfer admittance amplifier. (a) Actual transfer admittance amplifier. (b) Equivalent circuit representation for (a), showing characteristic misalignment generators E_M and I_M.

G_y = short circuit transfer admittance ratio
$G_y = -I_2/V_1$ with $M=0$, Z_L (Load) $= 0$
$Z_{in_i} =$ input impedance of ideal amplifier $= \infty$
$Z_{o_i} =$ output impedance of ideal amplifier $= \infty$
E_M = equivalent input misalignment voltage generator
I_M = equivalent input misalignment current generator.

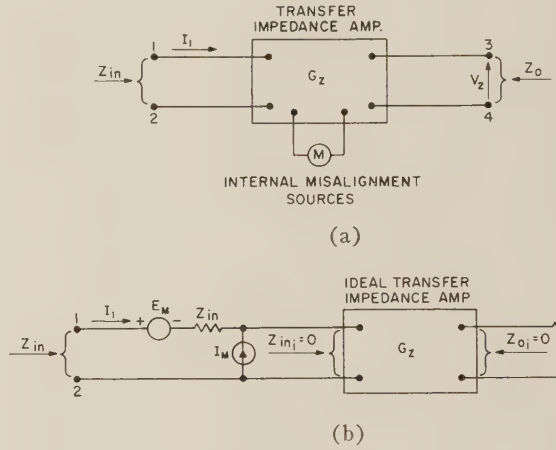


Fig. 4—Transfer impedance amplifier. (a) Actual transfer impedance amplifier. (b) Equivalent circuit representation for (a), showing characteristic misalignment generators E_M and I_M.

G_z = open circuit transfer impedance ratio
$G_z = V_2/I_1$ with $M=0$, Z_L (Load) $= \infty$
$Z_{in_i} =$ input impedance of ideal amplifier $= 0$
$Z_{o_i} =$ output impedance of ideal amplifier $= 0$
E_M = equivalent input misalignment voltage generator
I_M = equivalent input misalignment current generator.

4) In vacuum tube amplifiers: grid current and changes therein at input tube grid; velocity of emission potential changes in the input tube.
5) In transistor amplifiers: base current and changes therein, caused by temperature, at the input transistor base (assuming grounded emitter input stage); base-emitter potential changes in the input transistor; variations of static dc current gain with environment (particularly temperature).

Whatever the sources of misalignment resulting in E_M and I_M of Fig. 1, it is possible, in theory, to evaluate each of the latter quantities. For *each* source of misalignment a component of E_M exists which is mathematically or experimentally evaluated in the following manner (a practical method of evaluating E_M for an amplifier employed in a computing system is given in Section V):

1) Short circuit input terminals 1–2.
2) Calculate or observe the change in open circuit voltage across output terminals 3–4 (*i.e.*, with the load impedance, Z_L, disconnected) caused by the misalignment source acting in the circuit. Call this change E_{o_M}.
3) E_M is then: $E_M = E_{o_M}/G_v$, where G_v is the open circuit voltage transfer ratio of the amplifier.
4) As an alternative to steps 2) and 3) above, we may find E_M if we know the voltage gain between the amplifier input terminals and a convenient circuit

node *in the chain of amplification*, either at or following the node (*i.e.*, closer to the output stage) where the misalignment source occurs. In this case, evaluate the voltage change, caused by the misalignment source, at the convenient circuit node with amplifier input terminals 1–2 shorted, as in step 1), and divide this change by the voltage gain from the input terminals to this node; the result is E_M.

Steps 1) through 3) above apply in general; alternative steps 1) and 4) may be more convenient to apply in specific instances.

For *each* source of misalignment a component of I_M exists which is mathematically or experimentally evaluated in the following manner (a practical method of evaluating I_M for an amplifier employed in a computing system is given in Section V):

1) Short circuit input terminals 1–2.
2) Calculate or observe the short circuit current which flows out of input terminal 1 towards terminal 2. I_M is this short circuit current. I_M, it will be recognized, is the Norton equivalent current generator (caused by the misalignment source) seen looking into input terminals 1–2.
3) As an alternative to steps 1) and 2) above, we may find I_M by observing or calculating the open circuit voltage, caused by the misalignment source, seen looking into amplifier input terminals 1–2. I_M is then this open circuit voltage divided by Z_{in}, the amplifier input impedance. It will be recognized that the open circuit voltage caused by the misalignment source is the Thevenin equivalent voltage generator seen looking into input terminals 1–2.

E_M and I_M each represents the statistical sum of all effects caused by the various misalignment sources. In general, sources which give rise to E_M also give rise to I_M and vice versa; hence, components of E_M may be correlated to components of I_M.

In vacuum tube amplifiers, I_M is primarily caused by grid and leakage currents and changes therein at the input tube grid. E_M, on the other hand, is typically caused by velocity of emission potential changes of the input tube, power supply potential changes, and component value changes. In well-designed vacuum tube amplifiers, misalignment sources giving rise to components of I_M do not give rise (significantly) to components of E_M and vice versa. In the latter cases, components of I_M are, therefore, essentially independent of components of E_M.

In transistor amplifiers I_M is typically caused by the flow of base current (for a grounded emitter type stage) and changes therein caused by a) collector-base saturation and leakage current variations, b) variations in dc current gain, and c) changes in the base-emitter potential. The main source of these variations is the temperature environment. Unlike the vacuum tube case, however, some of the misalignment sources which give rise to components of I_M in the transistor case also give rise to components of E_M. That is, some components of I_M are correlated to some components of E_M. Sources a), b), and c) above are typical of those which give rise to components of both I_M and E_M. Sources of misalignment introduced at and beyond the first stage transistor collector circuit generally give rise to significant components of E_M but not I_M. However, those sources which are involved in some way with the first stage base and emitter circuits give rise to components of both I_M and E_M.

III. Characteristic Generators for an Amplifier with a Grounded Emitter Transistor Input Stage

Fig. 5 shows a grounded emitter type of transistor amplifier stage which might be used as the input stage of a dc operational amplifier. The stage contains some emitter degeneration (via R_e) and a source of bias by means of R_b and V_{cc}. R_b is initially adjusted so that the potential of Q_1 base, with respect to ground, is zero at room temperature. It is assumed that V_{cc} and $-V_{ee}$ supplies are well regulated, and that $R_b \gg Z_{in1}$. It is the purpose here to determine the components of the characteristic generators E_M and I_M (as in Fig. 6) which are caused by changes in the input stage transistor dc (static) current gain, collector-base saturation and leakage currents, and base-emitter potential caused by temperature. Biard and Matzen[5] have shown that changes in these quantities may be represented as in the transistor equivalent circuit shown in Fig. 7.

To evaluate E_M, apply steps 1) and 4) for finding E_M (see Section II) to the circuit of Fig. 5. We then obtain:

$$E_M = \Delta V_{BE}\left[\frac{|\alpha| r_c + r_b}{|\alpha| r_c - (r_e + R_e)}\right] + (\Delta I_{co} + \Delta\bar{\alpha} I_e) r_c \left[\frac{(r_e + R_e) + r_b}{|\alpha| r_c - (r_e + R_e)}\right]. \quad (1)$$

If $R_e = 0$, E_M given by (1) is the negative of Biard and Matzen's expression for Δv_1 given by their (8); their Δv_1 is the potential which must be applied at the amplifier input terminals to exactly balance E_M.

To evaluate I_M, apply step 3) for finding I_M (see Section II) to the circuit of Fig. 5. The input impedance, Z_{in1}, looking into the transistor between its base and ground is

$$Z_{in1} = r_b + \frac{(r_e + R_e)(r_c + Z_L)}{r_e + R_e + Z_L + r_c(1 - |\alpha|)}. \quad (2)$$

[5] J. R. Biard and W. T. Matzen, "Drift considerations in low-level direct-coupled transistor circuits," 1959 IRE National Convention Record, pt. 3, pp. 27–33.

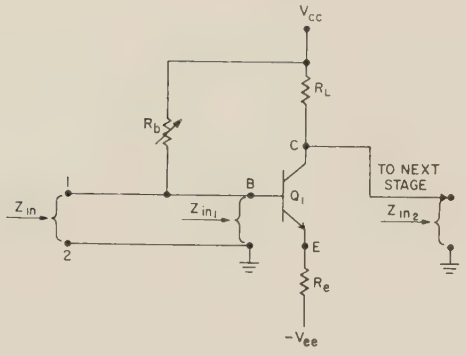


Fig. 5—Grounded-emitter transistor input stage.

Z_{in} = input impedance of stage
Z_{in_1} = input impedance of Q_1 (not including R_b)
Z_{in_2} = input impedance of next stage
$Z_L = (R_L Z_{in2})/(R_L + Z_{in_2})$ = effective collector load for Q_1.

The input impedance of the amplifier stage, Z_{in}, looking into its input terminals 1–2 is then

$$Z_{in} = \frac{R_b Z_{in1}}{R_b + Z_{in1}} \approx Z_{in1}, \qquad \text{since } R_b \gg Z_{in1}. \tag{3}$$

The Thevenin equivalent voltage generator, E_T, seen looking into the input terminals of the amplifier is (assuming $R_b \gg Z_{in1}$)

$$E_T = -\Delta V_{BE}\left[\frac{Z_L + r_c(1 - |\alpha|)}{r_e + R_e + Z_L + r_c(1 - |\alpha|)}\right] + (\Delta I_{co} + \Delta\bar{\alpha} I_e) r_c \left[\frac{r_e + R_e}{r_e + R_e + Z_L + r_c(1 - |\alpha|)}\right]. \tag{4}$$

I_M is then given by E_T/Z_{in}; this is,

$$I_M = -\Delta V_{BE}\left[\frac{Z_L + r_c(1 - |\alpha|)}{r_b[r_e + R_e + Z_L + r_c(1 - |\alpha|)] + (r_e + R_e)(r_c + Z_L)}\right] + (\Delta I_{co} + \Delta\bar{\alpha} I_e) r_c \left[\frac{r_e + R_e}{r_b[r_e + R_e + Z_L + r_c(1 - |\alpha|)] + (r_e + R_e)(r_c + Z_L)}\right]. \tag{5}$$

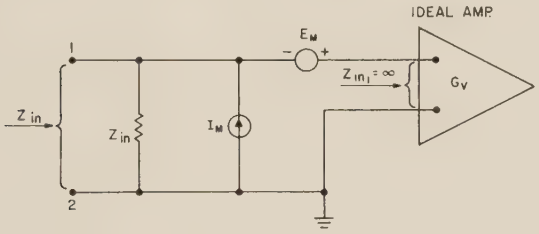


Fig. 6—Equivalent input circuit for transistor amplifier containing grounded-emitter input stage of Fig. 5.

G_v = open circuit voltage transfer ratio of actual amplifier
E_M = characteristic misalignment voltage generator
I_M = characteristic misalignment current generator.

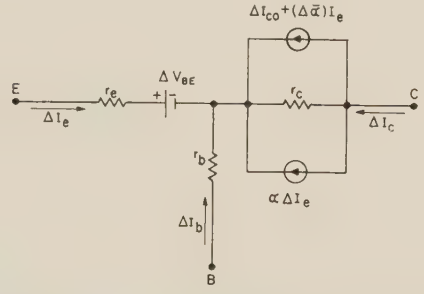


Fig. 7.—Small signal equivalent circuit of transistor.

I_e = emitter current at operating point
ΔI_e = change in emitter current
ΔI_b = change in base current
ΔI_c = change in collector current
ΔI_{co} = change in collector current caused by variations in collector-base diode saturation current and small signal collector resistance r_c.
ΔV_{BE} = change in base-emitter potential
α = small signal current transfer ratio ($\alpha < 0$)
$\Delta\bar{\alpha}$ = change in static (dc) value of current transfer ratio
r_e, r_b, r_c: small-signal equivalent "T" parameters of transistor.

If we assume

$$|\alpha| r_c \gg r_b, \qquad |\alpha| r_c \gg (r_e + R_e),$$
$$r_c(1 - |\alpha|) \gg (r_e + R_e + Z_L), \qquad r_c \gg Z_L,$$

then, (1), (3), and (5) above become, respectively:

$$E_M \approx \Delta V_{BE} + (\Delta I_{co} + \Delta\bar{\alpha} I_e)\left[\frac{r_e + R_e + r_b}{|\alpha|}\right], \tag{1a}$$

$$Z_{in} \approx r_b + \left[\frac{r_e + R_e}{1 - |\alpha|}\right], \tag{3a}$$

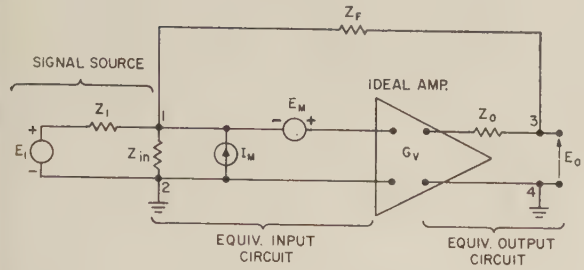
and

$$I_M \approx -\Delta V_{BE}\left[\frac{1 - |\alpha|}{r_e + R_e + r_b(1 - |\alpha|)}\right] + (\Delta I_{co} + \Delta\bar{\alpha} I_e)\left[\frac{r_e + R_e}{r_e + R_e + r_b(1 - |\alpha|)}\right]. \tag{5a}$$

Note that E_M and I_M both have components caused by ΔV_{BE} and $(\Delta I_{co} + \Delta\bar{\alpha} I_e)$.

IV. Misalignment in Computing Circuit Employing a DC Operational Amplifier

Fig. 8 shows a typical computing circuit employing a high-gain dc operational amplifier. The equivalent input and output circuits for the amplifier are shown and it is assumed that the various elements therein are known. If $|G_v|$ is sufficiently high (which is the usual case for good computing amplifiers), we can easily show



g. 8—Computing circuit with high gain dc operational amplifier.
E_1 = signal source voltage
Z_1 = signal source impedance
Z_f = feedback impedance
Z_{in} = input impedance of amplifier
Z_o = output impedance of amplifier
G_v = open circuit voltage transfer ratio
E_M, I_M: characteristic misalignment generators of amplifier.

at the output E_o (with but small error) is given by

$$E_o = -\left(\frac{Z_F}{Z_1}\right)E_1 - \left[1 + \frac{Z_F}{Z_1}\left(1 + \frac{Z_1}{Z_{in}}\right)\right]E_M - \left(\frac{Z_F}{Z_1}\right)Z_1 I_M \tag{6}$$

$$E_o = -\frac{Z_F}{Z_1}E_1 - E_{oM1} - E_{oM2}, \tag{6a}$$

here

$$E_{oM1} = \left[1 + \frac{Z_F}{Z_1}\left(1 + \frac{Z_1}{Z_{in}}\right)\right]E_M,$$

$$E_{oM2} = \left(\frac{Z_F}{Z_1}\right)Z_1 I_M.$$

The first term on the right of (6a) is the normal operational term for the signal; the second and third terms (E_{oM1} and E_{oM2}) represent the effects of the characteristic misalignment generators.

For a high gain transistorized dc amplifier containing grounded emitter input stage, as in Fig. 5, with E_M, Z_{in} and I_M given by (1a), (3a) and (5a), the misalignment terms E_{oM1}, and R_{oM2} become:

$$E_{oM1} = \left[1 + \frac{Z_F}{Z_1}\left[1 + \frac{Z_1}{r_b + \left(\frac{r_e + R_e}{1 - |\alpha|}\right)}\right]\right] \cdot \left[\Delta V_{BE} + (\Delta I_{co} + \Delta\bar{\alpha} I_e)\left(\frac{r_e + R_e + r_b}{|\alpha|}\right)\right] \tag{7}$$

$$E_{oM2} = -Z_F\left[\Delta V_{BE}\left[\frac{1 - |\alpha|}{r_e + R_e + r_b(1 - |\alpha|)}\right] - (\Delta I_{co} + \Delta\bar{\alpha} I_e)\left[\frac{r_e + R_e}{r_e + R_e + r_b(1 - |\alpha|)}\right]\right]. \tag{8}$$

If these misalignment terms are added together we obtain:

$$E_{oM1} + E_{oM2} = \Delta V_{BE}\left[1 + \frac{Z_F}{Z_1}\right] + (\Delta I_{co} + \Delta\bar{\alpha} I_e) \cdot \left[\frac{r_e + R_e + r_b}{|\alpha|}\right]\left[\frac{Z_F}{Z_1}\left(1 + \frac{Z_1}{r_e + R_e + r_b}\right) + 1\right]. \tag{9}$$

We deduce the following from (9), subject to the approximations made in obtaining (1a), (3a) and (5a):

1) Given ΔV_{BE}, and for a given operation (Z_F/Z_1), the output misalignment term involving ΔV_{BE} is fixed regardless of our choice of circuit constants.

2) For a given operation (Z_F/Z_1), the effect of the term involving $(\Delta I_{co} + \Delta\bar{\alpha} I_e)$ can be reduced by reducing Z_1. If:

a) $$\left|\frac{Z_1}{r_e + R_e + r_b}\right| \gg 1;$$

b) $$\left|\frac{Z_F}{Z_1}\left(\frac{Z_1}{r_e + R_e + r_b}\right)\right| \gg 1,$$

then changes in R_e do not significantly change the effect of the term involving $(\Delta I_{co} + \Delta\bar{\alpha} I_e)$. However, inasmuch as R_e affects the gain of the first stage, it is desirable to keep R_e small so that the stage gain is high and misalignments occurring after the first stage are make to look (effectively) small as regards their contributions to E_M. Assuming inequalities a) and b) above hold, (9) will reduce to

$$E_{oM1} + E_{oM2} = \Delta V_{BE}\left(1 + \frac{Z_F}{Z_1}\right) + (\Delta I_{co} + \Delta\bar{\alpha} I_e)\frac{Z_1}{|\alpha|}\left(\frac{Z_F}{Z_1}\right). \tag{9a}$$

It should be noted that the addition of chopper stabilization (via the Goldberg circuit) to the amplifier would reduce the misalignment term involving E_M by a factor of $(|A_c| + 1)$, where $|A_c|$ is the magnitude of the gain of the chopper amplifier.[6] However, the term involving I_M would be untouched. Assuming chopper stabilization reduced the E_M term to insignificance (*i.e.*, $E_{oM1} \approx 0$) then the output misalignment becomes just equal to $-E_{oM2}$. E_{oM2} may be written in the following form:

[6] E. A. Goldberg, "Stabilization of wide-band direct-current amplifiers for zero and gain," *RCA Rev.*, vol. 11, pp. 296–300; June, 1950.

$$E_{oM2} = -\Delta V_{BE}\left[\frac{Z_1(1-|\alpha|)}{r_e+R_e+r_b(1-|\alpha|)}\right]\left(\frac{Z_F}{Z_1}\right) + (\Delta I_{co}+\Delta\bar{\alpha}I_e)Z_1\left[\frac{r_e+R_e}{r_e+R_e+r_b(1-|\alpha|)}\right]\cdot\left(\frac{Z_F}{Z_1}\right). \quad (10)$$

Now the effect of ΔV_{BE} as well as that of $(\Delta I_{co}+\Delta\bar{\alpha}I_e)$ may be reduced by decreasing Z_1 for a given operation (Z_F/Z_1). However, if

$$\left|\frac{Z_1(1-|\alpha|)}{r_e+R_e+r_b(1-|\alpha|)}\right| \gg 1,$$

$$\left|\frac{Z_1}{r_e+R_e+r_b}\right| \gg 1,$$

the term involving ΔV_{BE} may now appear magnified compared to its value before chopper stabilization (depending upon the Z_F/Z_1 ratio). The term involving $(\Delta I_{co}+\Delta\bar{\alpha}I_e)$, however, is approximately the same order of magnitude as that before chopper stabilization. We thus arrive at the surprising fact that chopper stabilization, which is ordinarily employed to reduce misalignment effects, actually may increase the effective output misalignment rather than reduce it.

V. Practical Measurements of E_M and I_M for a Given Operational Amplifier

From the point of view of those in the computer field, E_M and I_M may be conveniently measured for a given operational amplifier by applying well-known computer techniques. Thus, in Fig. 8, if we set $E_1=0$, $Z_1=\infty$, $Z_F=0$, then from (6):

$$E_M = -E_{o1}, \quad (11)$$

where E_{o1} is the observed output under the stated test conditions.

If Z_{in} is known and we choose a particular value of Z_F, *e.g.*, a pure resistance R_F, and let $E_1=0$, $Z_1=\infty$, then I_M may be calculated from (6):

$$I_M = -\frac{1}{R_F}\left[E_{o2}+\left(1+\frac{R_F}{Z_{in}}\right)E_M\right], \quad (12)$$

where E_{o2} is the observed output under the stated conditions of test, and E_M is given by (11). Hence, if a particular environment (such as temperature, power supply potentials) is changed, the effects on E_M and I_M may be observed, and from (6) we may assess the relative importance of the misalignment terms on the output for a given operation (Z_F/Z_1). In this way the relative merits of two different operational amplifiers, either of which may be employed in a particular computing system, may be assessed with regard to misalignment.

VI. Characteristic Noise Generators

A pair of characteristic noise generators, E_N and I_N, analogous to the characteristic misalignment generators E_M and I_M, respectively, also exist for any amplifier provided that the original assumptions employed in showing the existence of E_M and I_M hold true at noise frequencies. These noise generators may be defined analogously to the way E_M and I_M were defined. In general, components of E_N and I_N, caused by any particular internal noise source, are correlated. As for the case of the characteristic misalignment generators, E_N and I_N each represents the statistical sum of all components. Computer techniques, similar to those used for measuring E_M and I_M [via (11) and (12)] may also be used to find E_N and I_N. However, the phase relations between noise frequency components of both E_N and I_N must be reckoned with in employing an equation similar to (12). Furthermore, if noise components are random and cannot be isolated, the terms on the right side of (12) generally do not add on a linear basis as (12) indicates. Hence, representation of amplifier internal noise by characteristic noise generators may be a complicated process. Fortunately, in many cases noise sources giving rise to components of E_N do not give rise to significant components of I_N, and vice versa that is, E_N and I_N are essentially uncorrelated. In these cases, the rms values of the characteristic noise generators may be evaluated via (11) and (12), taking care to add the terms in (12) on a squared, rather than linear, basis. The E_N and I_N generators found in this way can be useful in assessing the effects of noise on a computing system. It should be pointed out that noise introduced into the amplifier by environment (such as power supply noise, for example) as well as normal (inherent) noise existing in the amplifier (caused by noisy circuit components), may be represented by the components of the equivalent input characteristic noise generators E_N and I_N.

A Feedback Method for Obtaining a Synchro Output Signal Proportional to Input Angle ⊖ for Large ⊖*

M. B. BROUGHTON†, MEMBER, IRE

Summary—If the ac signal at the "cosine" terminal of a sine-osine resolver (or synchro transmitter connected to a transformer o as to perform the function of a sine-cosine resolver) is fed back o the rotor through an amplifier of suitable gain, the signal at the sine" terminal can be made proportional to rotor rotation for angles p to 90° or greater. A theoretical analysis of the relationship

$$\theta \doteq \frac{\sin\theta}{a + b\cos\theta}$$

s given, along with a method for deriving its analog. The theoretical evelopment is supported by experiment.

Introduction

A CERTAIN design required that the voltage from the output of a synchro transmitter be proportional to the angle of shaft rotation instead of the sine of this angle, as is the case in one of its more usual configurations. Technical and temporal considerations precluded the change to linear resistance or induction potentiometer pickoffs. It was, therefore, decided to explore the possibilities of improving upon the approximation of θ by $\sin\theta$, good only at small angles, through the use of feedback. The remainder of this paper is devoted to theory, design considerations, and an experimental illustration of a feedback method of providing a synchro output voltage proportional to shaft rotation θ for large θ.

Theory

If an output proportional to $\cos\theta$ could be obtained, then the expression most likely realizable by feedback methods is

$$\frac{\sin\theta}{a + b\cos\theta}.$$

If the appropriate series are substituted for $\sin\theta_0$ and $\cos\theta$ in the above, one obtains

$$\frac{\sin\theta}{a + b\cos\theta} = \frac{\theta - \dfrac{\theta^3}{3!} + \cdots}{a + b\left[1 - \dfrac{\theta^2}{2!} + \cdots\right]}$$

$$= \frac{\theta - \dfrac{\theta^3}{3} + \cdots}{(a+b)\left[1 - \dfrac{b}{a+b}\dfrac{\theta^2}{2!} + \cdots\right]}$$

$$= \frac{\left[\theta - \dfrac{\theta^3}{3!} + \cdots\right]\left[1 + \dfrac{b}{a+b}\dfrac{\theta^2}{2} + \cdots\right]}{a+b}$$

$$= \frac{\theta}{a+b} + \frac{\theta^3}{a+b}\left[\frac{b}{(a+b)2!} - \frac{1}{3!}\right] + \cdots.$$

Requiring that the coefficients of θ and θ^3 be one and zero respectively, yields

$$a = \tfrac{2}{3}, \qquad b = \tfrac{1}{3}.$$

Substituting these values and plotting

$$\theta - \frac{\sin\theta}{\frac{2}{3} + \frac{1}{3}\cos\theta}$$

clearly shows that the error is less than that for the relation $\theta - \sin\theta$. These two error expressions are compared in Fig. 1.

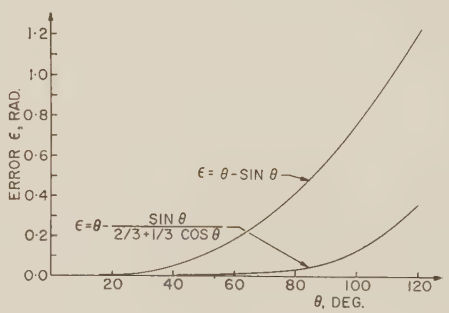


Fig. 1—Graph of error vs angle θ for two approximations of θ.

Having concluded that the approximation

$$\theta \doteq \frac{\sin\theta}{a + b\cos\theta} \tag{1}$$

is a worthwhile improvement over the better known small angle relation $\theta \doteq \sin\theta$, it remains to select a and b according to some optimization criterion in order that the inherent error be minimized. Such criteria as least error magnitude, zero error at certain values of θ, and others, may be dictated by system requirements, but the one selected for illustration here is that of least square error over the interval of interest, $-L$ to $+L$. Since the value of the error for $\theta < 0$ is simply minus the

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error for $\theta>0$, examination over the interval from 0 to $+L$ is adequate.

Mathematically, for minimization of the least square error, values of a and b which satisfy

$$\frac{\partial}{\partial a}\int_0^L\left[\theta-\frac{\sin\theta}{a+b\cos}\right]^2 d\theta=0 \tag{2}$$

and

$$\frac{\partial}{\partial b}\int_0^L\left[\theta-\frac{\sin\theta}{a+b\cos\theta}\right]^2 d\theta=0 \tag{3}$$

must be found.

If (2) and (3) are attempted as they stand, integrands of the form

$$\frac{\theta\sin\theta}{a+b\cos\theta}$$

will be encountered. Since these are not generally integrable in closed form, it was decided instead to find the values of a and b which solved

$$\frac{\partial}{\partial a}\int_0^L[(a+b\cos\theta)\theta-\sin\theta]^2 d\theta=0 \tag{4}$$

and

$$\frac{\partial}{\partial b}\int_0^L[(a+b\cos\theta)\theta-\sin\theta]^2 d\theta=0. \tag{5}$$

This was justified by arguing that $a+b\cos\theta$ was not a strong function of L.[1] After the operations indicated in (4) and (5) are completed, there result the following simultaneous equations whose solution yields a and b:

$$\frac{L^3}{3}a+(L^2\sin L+2L\cos L-2\sin L)\times b = \sin L-L\cos L \tag{6}$$

and

$$(L^2\sin L+2L\cos L-2\sin L)\times a+\left(\frac{L^3}{6}+\frac{L^2}{4}\sin 2L+\frac{L}{4}\cos 2L-\frac{1}{8}\sin 2L\right)\times b=\frac{1}{8}\sin 2L-\frac{L}{4}\cos 2L. \tag{7}$$

As functions of L, a and b are plotted in Figs. 2 and 3, respectively. Clearly, a and b do not change rapidly with changes in L, thus supporting the assumption made when (4) and (5) were written down.

It is instructive to examine the magnitude of the theoretical deviation from the desired linear relationship as given by the equation

$$\epsilon=\theta-\frac{\sin\theta}{a(L)+b(L)\cos\theta}, \tag{8}$$

for particular values of L.

[1] A solution of (2) and (3) is now in progress.

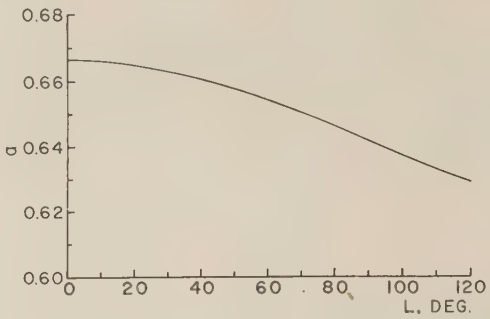

Fig. 2—Parameter a vs upper limit L.

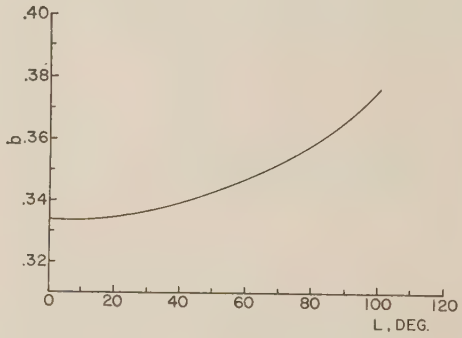

Fig. 3—Parameter b vs upper limit L.

The solution of $d\epsilon/d\theta=0$ results in the quadratic equation in $\cos\theta$: $a\cos 0+b=(a+b\cos\theta)^2$, whose solution yields two values of θ, designated θ_M^- and θ_M^+, which are plotted as functions of L in Fig. 4. A third error peak will occur at L. The magnitudes of the three peak errors, occurring at θ_M^-, θ_M^+ and L, are obtained by substitution in (8), and are plotted in Fig. 5. These are seen to be quite small, even for angles as large as 90°, where the maximum deviation is only about 0.011 radian.

There remains the physical realization of the relationship expressed by (1). An analysis of the network of Fig. 6 will show that the output voltage is the analog of (1), subject to restraints to be derived. It should be pointed out that the synchro transmitter-transformer combination could be replaced by a resolver, without altering the general nature of the derivation.[2] With reference to the circuit of Fig. 6, the following nomenclature will be employed:

Z_1, Z_2, Z are the input, feedback, and rotor impedances, respectively; E, E_1, E_{out} are the input, rotor, and output voltages, respectively; k is the transformation ratio between the primary (rotor) and any stator winding; k' is the transformer voltage ratio; K is the magnitude of the amplifier gain; θ is the rotor rotation from the position which gives zero output at the "sine" terminal.

For the synchro-transformer configuration in Fig. 6, it can be shown that the signal at the transformer center

[2] B. Chance, *et al.*, "Waveforms," M.I.T. Rad. Lab. Ser., McGraw-Hill Book Co., Inc., New York, N. Y., vol. 19, p. 444; 1949.

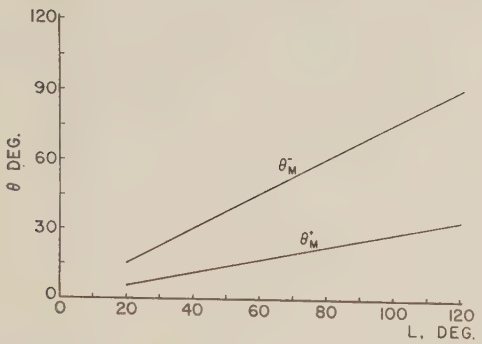

Fig. 4—θ^+ and θ^- vs upper limit L.

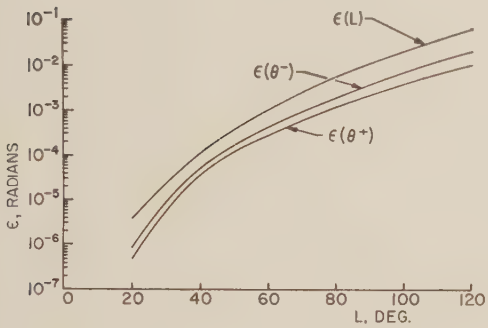

Fig. 5—$\epsilon(\theta^+)$, $\epsilon(\theta^-)$, $\epsilon(L)$, vs upper limit L.

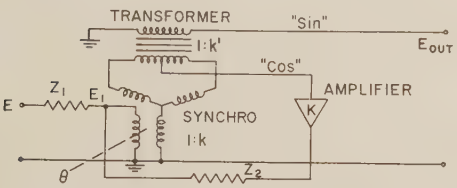

Fig. 6—Feedback circuit makes synchro output proportional to θ.

tap is $2k \cos\theta$ times the input voltage, while that at the transformer secondary is $\sqrt{3}kk' \sin\theta$ times the input voltage. If we apply Kirchhoff's current law, the current in the synchro rotor is

$$\frac{E_1}{Z} = \frac{E - E_1}{Z_1} + \frac{2kKE_1 \cos\theta - E_1}{Z_2} \tag{9}$$

whence,

$$E_1 = \frac{E}{1 + \frac{Z_1}{Z} + \frac{Z_1}{Z_2}(1 - 2kK\cos\theta)} \tag{10}$$

and the output signal is

$$E_{out} = \frac{\sqrt{3}kk'E\sin\theta}{1 + \frac{Z_1}{Z} + \frac{Z_1}{Z_2} - 2kK\frac{Z_1}{Z_2}\cos\theta}. \tag{11}$$

Eq. (11) can be written

$$E_{out} = \frac{E\sin\theta}{\left[1 + \frac{Z_1}{Z} + \frac{Z_1}{Z_2}\right]\frac{1}{\sqrt{3}kk'} - \frac{2}{\sqrt{3}}\frac{K}{k'}\frac{Z_1}{Z_2}}\cos\theta. \tag{12}$$

Now, equating the coefficients of the denominator of (12) to a and b of (1), one obtains

$$\left[1 + \frac{Z_1}{Z} + \frac{Z_1}{Z_2}\right]\frac{1}{\sqrt{3}kk'} = a, \tag{13}$$

and

$$\frac{-2}{\sqrt{3}}\frac{K}{k'}\frac{Z_1}{Z_2} = b. \tag{14}$$

In any given instance, a and b are specified as functions of the limit L of the region of interest; k, k', and Z depend upon the components available, and hence are not generally variable. Thus, there remains the determination of Z_1, Z_2, and K. One of these can be specified by such a criterion as amplifier capability, or supply voltage limitations, for example, and (13) and (14) solved for the other two. Note that solutions do not always exist for all possible parameter combinations. Z is, in general, a complex quantity and hence, Z_1 and Z_2 will also be complex. However, if the synchro primary is "tuned," Z_1 and Z_2 can be realized using resistors only. The design may now be considered complete.

As was pointed out above, the synchro-transformer combination of Fig. 6 could be replaced by a resolver, without affecting the validity of the analysis. However, the parameter k', the transformer voltage ratio, is no longer a design factor. Eqs. (13) and (14) may now be written

$$1 + \frac{Z_1}{Z} + \frac{Z_1}{Z_2} = ka \tag{15}$$

and

$$\frac{-KZ_1}{Z_2} = b. \tag{16}$$

Now, for real Z_1 and Z_2, $ka > 1$. Since $k < 1$ and $a < 1$, this requirement can only be met by making the overall voltage gain from input to output less than unity.

A gain factor of $n(n < 1)$ can be chosen to make Z_1 and Z_2 real, and (15) and (16) become

$$1 + \frac{Z_1}{Z} + \frac{Z_1}{Z_2} = \frac{k}{n}a \tag{17}$$

and

$$\frac{-KZ_1}{Z_2} = \frac{b}{n}. \tag{18}$$

Experimental Results

A Reeves type R 600 resolver, model one zero, was selected to provide experimental verification of the design procedures described above. Its measured values of impedance at 400~ and transformation ratio were $Z = 19{,}850$ ohms and $k = 0.935$, respectively. The phase shift between rotor and stator windings was about 3°.

No attempt was made to eliminate this slight amount of phase shift.

It was decided to determine the output deviation from linearity over the region $-90°$ to $+90°$. From Figs. 2 and 3, a and b were determined as 0.6415 and 0.3670, respectively: n was chosen as $\frac{1}{3}$, and Z_1 was a precision resistor whose measured resistance was 2230 ohms. Substituting these values in (17) and (18) gave $Z_2 = 3195$ ohms, and the amplifier gain $K = -1.600$.

The experimental and theoretical deviations from the desired linear relationship between input angle θ and output signal are compared in Fig. 7. Although no attempt was made to do so, it is believed that the rms deviation in the experimental case could have been reduced somewhat by slight parameter adjustments. Nevertheless, it is evident that the experimental results verify the theoretical developments above.

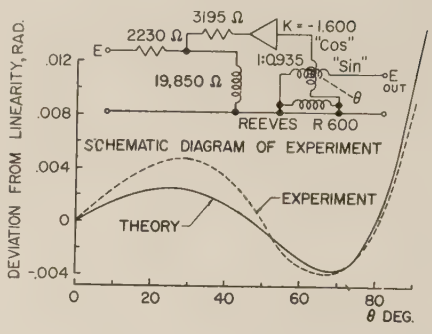

Fig. 7—Comparison of theoretical and experimental deviations from linearity.

Conclusions

An improved approximation to an angle θ, suitable for large-angle use, has been derived, and its theoretical errors have been examined. A comparatively straightforward realization of this approximation has been obtained using feedback around either a synchro or sine-cosine resolver. Experimental results have supported the theoretical analysis. The effect of parameter changes on the output linearity was not examined.

Acknowledgment

The author is grateful for the mathematical and technical assistance provided by I. Connell, J. Belanger, and J. Baril.

A Solution to the Euler Angle Transformation Equations*

GILBERT R. GRADO†

Summary—**As simulation studies grow more elaborate and complex, the computer operator is confronted with an ever increasing number of problems not directly associated with the study at hand. This paper describes a specially designed computer for solving the coordinate transformation equations normally encountered in a six degree of freedom simulation study. This computer expands the capabilities of present analog computer consoles and eliminates the tedious task of patching the solution to these equations, while eliminating a source of human error. Besides incorporating several unique features for changing sequences and scales, this machine has accuracies and responses compatible with those found in linear equipment.**

I. Introduction

In recent years the need for more comprehensive simulation studies has been accentuated by the complexities associated with weapon systems synthesis and analysis. This need has resulted in a greater amount of computational equipment required for a suitable solution, as well as a greater effort by the analyst to assure correct results. Whereas in the past, the breakdown of a system into block diagrams for two-dimensional models was quite simple and straightforward, the advent of three-dimensional simulation introduced more complex angular relationships (Fig. 1). These effects are quite difficult to visualize, and the part that man's intuition plays in trouble-shooting a problem is considerably reduced. Not only are equipment and mathematical faults more difficult to locate, but all too often mistakes in one's intuition will lead to a long search for a nonexistent trouble.

To counter these difficulties, many engineers and mathematicians in the analog simulation field have resorted to setting up their problems from a block diagram viewpoint. In this manner the transfer function associated with each block can be determined, and the response to a given input will be known, thereby, each block can be quickly and completely analyzed and a fault suspected to exist in a certain block can be readily isolated. This method preserves the system concept and

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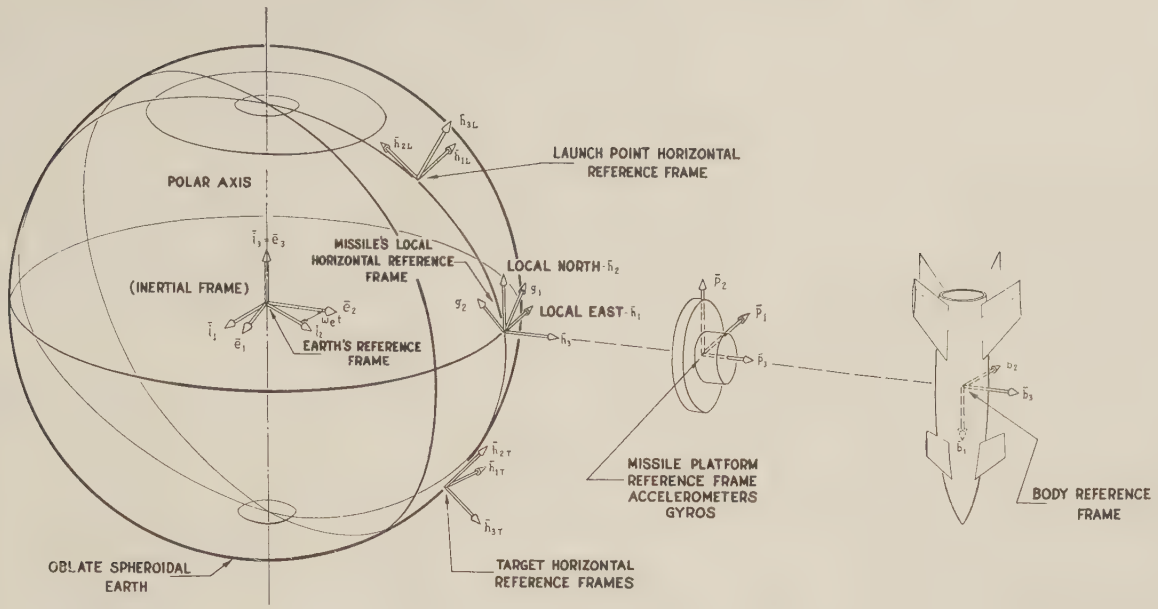

Fig. 1—Reference frames.

rovides a closer analogy between the simulated and ctual systems.

A further study of the functional block diagram reeals that a major portion of a three-dimensional, six egrees of freedom, missile study consists of the angular elationships between the various reference frames (Fig.). This is to be expected since in the weapon system he guided missile is automatically vectored to a target. Furthermore, in simulation studies certain types of coordinate transformations are required which, in actual light, are achieved physically. It was the constant reurrence of these transformation equations in every issile study that led the Flight Simulation Laboratory o develop a piece of equipment specifically programmed or solving these equations.

II. Euler Angle Transformation Operations

Before we become too involved with the equipment etails, let us briefly review the transformation equaions (Fig. 3, page 365). One reference frame may be niquely oriented with respect to a second reference rame through three ordered angles.[1,2] The Euler angles ncountered are of two types:

1) Repetitive Euler angles as used in classical mehanics in which one of the three angular rotations is reeated, and a line of nodes is established, *e.g.*, the three rdered rotations might be yaw, roll, yaw.

2) Successive Euler angles in which none of the rotaions are repeated, *e.g.*, yaw, pitch, roll. The first rotaion is about an axis of the initial reference frame, the hird of the ordered rotations about an axis of the final reference frame, and the second rotation is about an axis normal to the first and third rotation axes.

Since the gimballed body pickoff angles, as encountered in gyros, stable platforms, and radar antennas, are of the successive type and consequently used extensively in missile equations of motion, this will be the type referred to exclusively in this paper.[3]

The Euler angles are normally designated by ϕ, θ, ψ, where the correspondence is such that ϕ, θ, ψ, are always associated with rotations about the $\overline{R}_{1j}$, $\overline{R}_{2j}$, $\overline{R}_{3j}$ $(j=1, 2, 3)$ vectors, respectively.[4] The subscript $1j$, *e.g.*, indicates the $\overline{R}_1$ axis after the jth rotation. The total number of ordered sets or sequences of Euler angles is given by the permutations of three angles taken three at a time, or six. The sequences of rotation are as follows:

$$\begin{array}{lll} \phi & \theta & \psi \\ \theta & \psi & \phi \\ \psi & \phi & \theta \\ \phi & \psi & \theta \\ \psi & \theta & \phi \\ \theta & \phi & \psi. \end{array}$$

The Euler angles represent an ordered triple of numbers; thus for a unique orientation of one frame R_i, with respect to a second frame F_i, the angles ψ_1, θ_1, ϕ_1, for the sequence yaw, pitch, roll will have different numerical values than the angles ψ_2, ϕ_2, θ_2 for the sequence yaw, roll, pitch. Therefore, unless an Euler sequence is specified, the three commonly denoted angles of yaw, pitch, and roll are ambiguous.

[1] B. Etkin, "Dynamics of Flight," John Wiley & Sons, Inc., New ork, N. Y.; 1959.

[2] W. J. Duncan, "Control and Stability of the Aircraft," Camridge Aeronautical Ser., Cambridge University Press, Cambridge, ngland; 1952.

[3] "Proceedings of First Flight Simulation Symposium," White Sands Missile Range, N. M., Special Rept., No. 9; November, 1957.

[4] J. Pappas, "Mathematical Modeling for Missile Systems," White Sands Missile Range, N. M., Special Rept. No. 13; March, 1959.

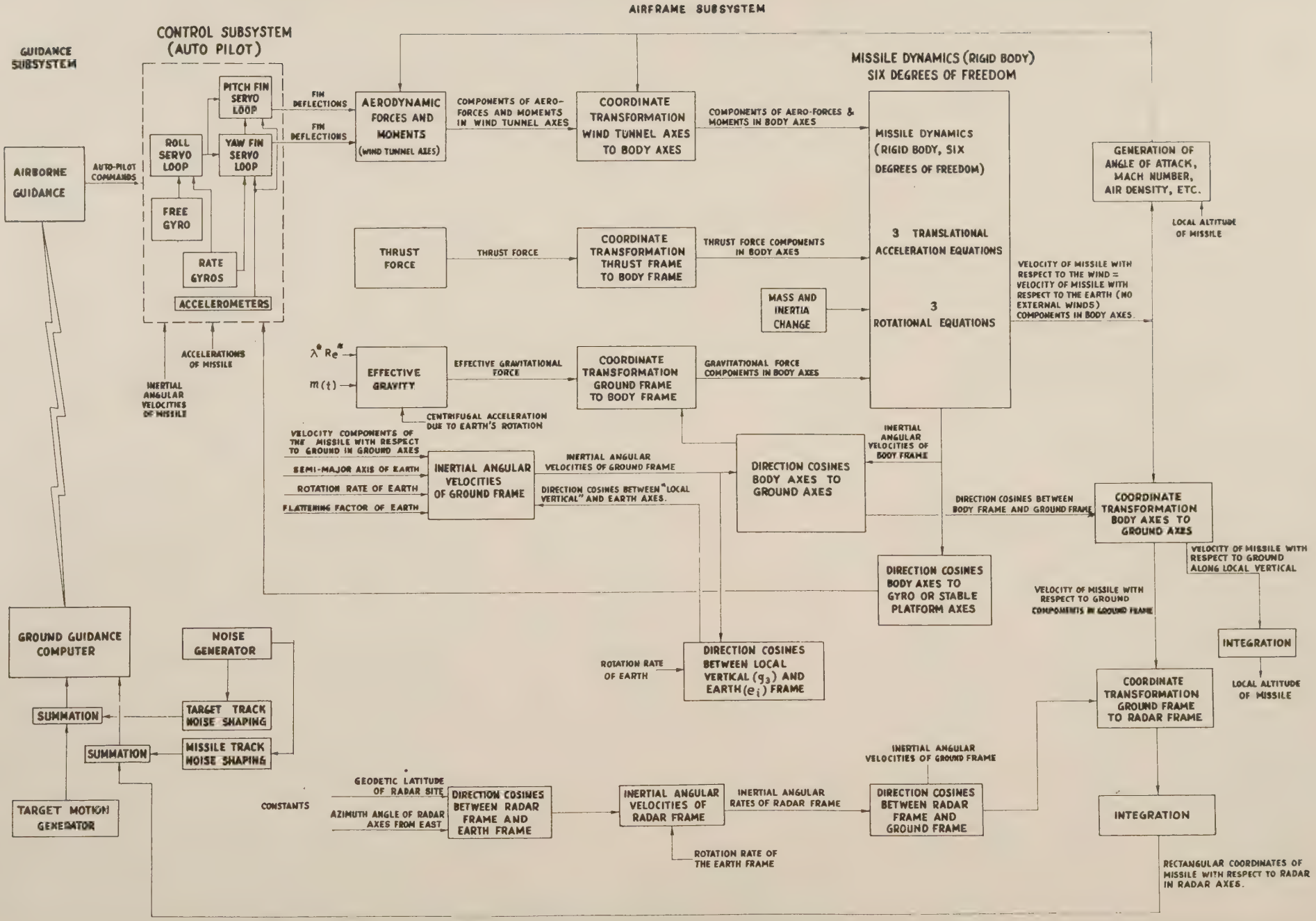

Fig. 2—Block diagram of a simulated missile system.

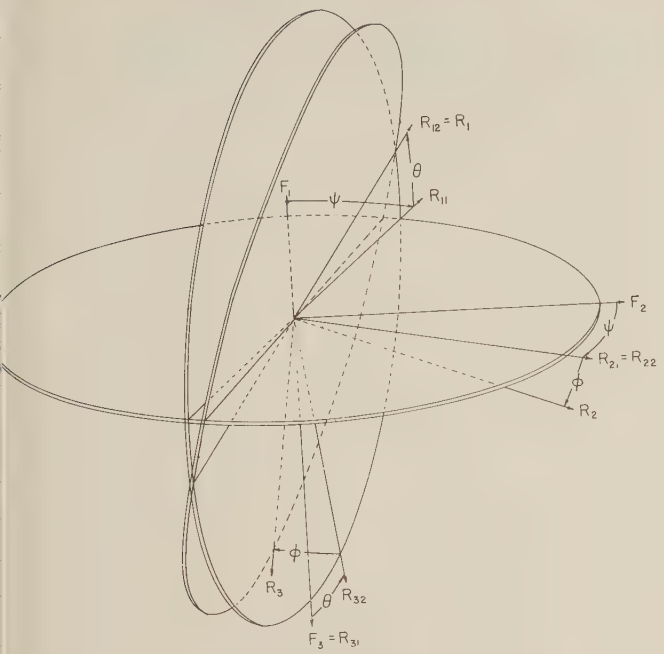

Fig. 3—Euler angle sequence ψ, θ, ϕ.

The derivation of the Euler angle equations is accomplished in the following manner. A unit vector $\overline{R}_1$ can be positively identified by three angles α_1, β_1, γ_1, (Fig. 4). Similarly, the vectors $\overline{R}_2$ and $\overline{R}_3$ can be identified with angles α_2, β_2, γ_2, and α_3, β_3, and γ_3, respectively. The angle α_j is the angle between $\overline{F}_1$ and $\overline{R}_j$; β_k is the angle between $\overline{F}_2$ and $\overline{R}_k$, and γ_L is the angle between $\overline{F}_3$ and $\overline{R}_L$. The resultant equations can be expressed in the general matrix form:

$$\begin{pmatrix} \overline{R}_1 \\ \overline{R}_2 \\ \overline{R}_3 \end{pmatrix} = \begin{pmatrix} \cos\alpha_1 & \cos\beta_1 & \cos\gamma_1 \\ \cos\alpha_2 & \cos\beta_2 & \cos\gamma_2 \\ \cos\alpha_3 & \cos\beta_3 & \cos\gamma_3 \end{pmatrix} \begin{pmatrix} \overline{F}_1 \\ \overline{F}_2 \\ \overline{F}_3 \end{pmatrix}.$$

In particular, if a rotation is performed only about $\overline{F}_1$, then the resultant matrix is

$$M_\phi = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\phi & \sin\phi \\ 0 & -\sin\phi & \cos\phi \end{pmatrix},$$

where ϕ is the angle of rotation about the $\overline{F}_1$ axis in a positive direction assuming a right hand coordinate system. In a similar manner, the matrix for the rotation about the $\overline{F}_2$ axis is

$$M_\theta = \begin{pmatrix} \cos\theta & 0 & -\sin\theta \\ 0 & 1 & 0 \\ \sin\theta & 0 & \cos\theta \end{pmatrix},$$

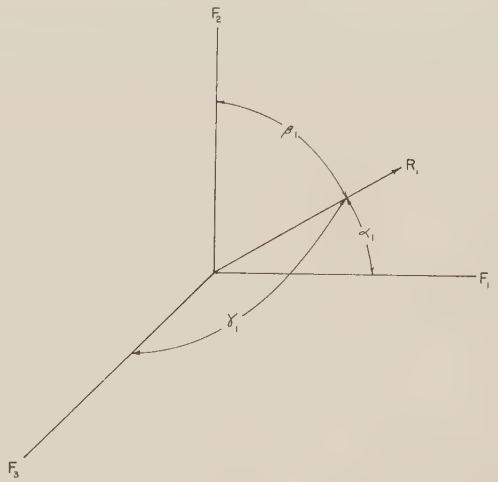

Fig. 4—Direction angles between R_1 and fixed frame.

where θ is the angle of rotation about $\overline{F}_2$ axis, and the matrix for the rotation about the $\overline{F}_3$ axis is

$$M_\psi = \begin{pmatrix} \cos\psi & \sin\psi & 0 \\ -\sin\psi & \cos\psi & 0 \\ 0 & 0 & 1 \end{pmatrix},$$

where ψ is the angle of rotation about the $\overline{F}_3$ axis.

The direction cosine matrix for any of the six sequences can now be calculated. For instance, the direction cosine matrix for the first sequence: ϕ, θ, ψ consists of the following multiplication $M_\psi \cdot M_\theta \cdot M_\phi$, so that

$$\begin{pmatrix} \overline{R}_1 \\ \overline{R}_2 \\ \overline{R}_3 \end{pmatrix} = \begin{pmatrix} \cos\theta\cos\psi & \cos\phi\sin\psi + \sin\phi\sin\theta\cos\psi & \sin\phi\sin\psi - \cos\phi\sin\theta\cos\psi \\ -\cos\theta\sin\psi & \cos\phi\cos\psi - \sin\phi\sin\theta\sin\psi & \sin\phi\cos\psi + \cos\phi\sin\theta\sin\psi \\ \sin\theta & -\sin\phi\cos\theta & \cos\phi\cos\theta \end{pmatrix} \begin{pmatrix} \overline{F}_1 \\ \overline{F}_2 \\ \overline{F}_3 \end{pmatrix}.$$

In a similar manner, the transformation matrices for the other five sequences can be derived. It is to be noted that the frame $\overline{R}_1$ is rotated with respect to $\overline{F}_1$ through positive angles. Thus when particular vectors are substituted into the equations, the frame which is being oriented through the Euler angles, with respect to a second frame, should be put in the left hand side of the equation. If not, rows and columns of the direction cosine matrices should be interchanged, as well as the signs of the Euler angles changed, since reversing the transformations (going from the $\overline{R}_1$ frame backwards to the $\overline{F}_1$ frame through the same magnitudes of angles) requires negative angles.

In the simulation of the guided missile system it also becomes necessary to generate the Euler angles. The information available consists of the initial angles plus the relative angular velocities of the rotating frame with respect to the fixed reference frame. Missile studies up to the present use the fixed reference frame as an inertial frame, thus the equations relating the motions between the rotating and fixed coordinate systems can be derived

for each of the sequences in a simplified fashion. The equations for the sequence ϕ, θ, ψ, are shown below:

$$\dot{\phi} = \sec\theta(P\cos\psi - Q\sin\psi)$$

$$\dot{\theta} = Q\cos\psi + R\sin\psi$$

$$\dot{\psi} = +R - \tan\theta(P\cos\psi - Q\sin\psi).$$

Similarly, the equations for the sequence ψ, θ, ϕ can be derived,

$$\dot{\psi} = \sec\theta(R\cos\phi + Q\sin\phi)$$

$$\dot{\theta} = Q\cos\phi - R\sin\phi$$

$$\dot{\phi} = P + \tan\theta(R\cos\phi + Q\sin\phi),$$

and so on for the other remaining four sequences.

Upon examination of the direction cosine matrices for the various sequences, a definite pattern is detected. This is to be expected since the same sequence of events is effected in each case. There is a rotation about an axis of the first reference frame, a second rotation about an axis normal to the first and third rotation axes, and a third rotation about an axis of the final reference frame. Even though the angles are referred to by different names, and the axes numbered in a different manner, the procedures in going from one reference frame to another is basically the same, regardless of the sequence. A particular sequence merely assigns specific names to the three ordered angles of rotation. This point is illustrated in Table I, which results from this study.

ing from one Euler angle sequence to another. This means that a general form for the equations could be derived in terms of the angles in the sequence and the orientation of the axes. Since the primary objective was to develop the equipment as soon as possible, and the conversion table gave all of the necessary information for designing the equipment, the derivation of a general form of the Euler angle equations was put off to a later date.

III. Description of Equipment

In describing the operation of the equipment we will refer to the sequence of yaw, pitch, roll (ψ, θ, ϕ) for convenience. This happens to be the most frequently used sequence,[1] and the transformation to any other sequence is easily accomplished with the use of the conversion table.

The equipment performs three basic functions. The first section generates the sines and cosines of the three Euler angles by satisfying the differential equations previously mentioned. The second increment produces the nine elements of the direction cosine matrix from the sines and cosines of the Euler angles. The third unit multiplies three orthogonal vectors in the rotating frame by the corresponding elements in the matrix to transform these vectors to the fixed reference frame. In a typical missile application, the velocities along the three ground frame axes are obtained in terms of the velocity components along the missile body axes. The equipment is a self-contained package with all signal, reference, and

TABLE I

$\phi\ \theta\ -\psi$	$P\ Q\ -R$	$U\ V\ -W$	$\dot{X}\ \dot{Y}\ -\dot{Z}$	$a_{11}\ a_{12}\ -a_{13}\ a_{21}\ a_{22}\ -a_{23}\ -a_{31}\ -a_{32}\ a_{33}$
$\theta\ \psi\ -\phi$	$Q\ R\ -P$	$V\ W\ -U$	$\dot{Y}\ \dot{Z}\ -\dot{X}$	$a_{22}\ a_{23}\ -a_{21}\ a_{32}\ a_{33}\ -a_{31}\ -a_{12}\ -a_{13}\ a_{11}$
$\psi\ \phi\ -\theta$	$R\ P\ -Q$	$W\ U\ -V$	$\dot{Z}\ \dot{X}\ -\dot{Y}$	$a_{33}\ a_{31}\ -a_{32}\ a_{13}\ a_{11}\ -a_{12}\ -a_{23}\ -a_{21}\ a_{22}$
$\phi\ \psi\ \theta$	$P\ R\ Q$	$U\ W\ V$	$\dot{X}\ \dot{Z}\ \dot{Y}$	$a_{11}\ a_{13}\ a_{12}\ a_{31}\ a_{33}\ a_{32}\ a_{21}\ a_{23}\ a_{22}$
$\psi\ \theta\ \phi$	$R\ Q\ P$	$W\ V\ U$	$\dot{Z}\ \dot{Y}\ \dot{X}$	$a_{33}\ a_{32}\ a_{31}\ a_{23}\ a_{22}\ a_{21}\ a_{13}\ a_{12}\ a_{11}$
$\theta\ \phi\ \psi$	$Q\ P\ R$	$V\ U\ W$	$\dot{Y}\ \dot{X}\ \dot{Z}$	$a_{22}\ a_{21}\ a_{23}\ a_{12}\ a_{11}\ a_{13}\ a_{32}\ a_{31}\ a_{33}$

Table I lists the angles in the proper sequence at the left while the rest of the table contains all the other terms appearing in the equations to be solved by this equipment. U, V, and W are the translational velocities along the missile or rotating axes; while $\dot{X}$, $\dot{Y}$ and $\dot{Z}$ represent the resultant velocity components on the ground or fixed coordinate frame. The terms P, Q and R denote the angular velocities about the $\overline{R}_1$, $\overline{R}_2$, and $\overline{R}_3$ axes, respectively. The terms shown at the right side of Table I represent the matrix elements of the equations. The negative signs are required to satisfy the change from a reverse cyclic group to the forward cyclic groups, represented by the first three sequences. Interchanging of the terms in any row by the corresponding terms in another row will yield the equations for the new sequence.

The interchangeability of terms in both the direction cosine matrix and the differential equations for the generation of the Euler angles is thus established for changing

operating voltages terminated in one connector. The Euler Angle Computer is incorporated as part of an Electronic Associates Type 231R computer. The patch board termination area, shown in Figs. 5 and 6, can be covered by any one of six interchangeable decals, each designating the connections for one of the six possible sequences. The variation in hole designations from one sequence to another was determined by the conversion table. The sequence in each decal is determined by the order of the angles in the upper left hand corner. Looking at the figure of the decal, one also sees that the Euler Angle Computer is fully controlled through the patch board in the control console. Hold and reset relays are brought out to the patchbay so that the Euler Angle Computer can be slaved to the main computer, if so desired. Various rate scale and range scale relays can be actuated for different problems, and the operation of these circuits will be fully explained in the next four paragraphs.

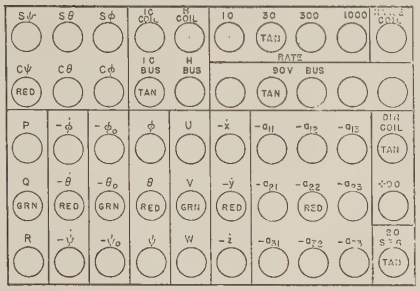

Fig. 5—Patch panel overlay for ψ, θ, ϕ sequence.

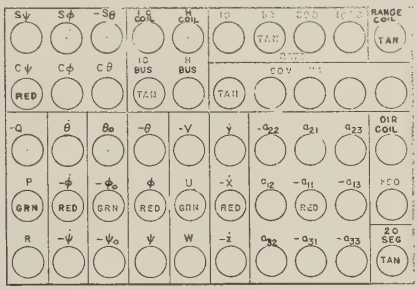

Fig. 6—Patch panel overlay for ψ, ϕ, θ sequence.

The Euler Angle Computer was designed with this thought in mind, achieving the utmost in speed and accuracy, without major component developments. Linear equipment presented no problems, while the electronic multipliers using the time division principle provided the necessary accuracies. Therefore, the only item to be developed was a suitable sine-cosine generator. This problem was overcome by using a sine generator of the diode function type. By distributing the break points at approximately 6° intervals, the device will provide accuracies within 0.01 per cent up to 30°, and within 0.02 per cent up to 90°. This means then that the best accuracy is obtained around zero output where the need is greatest, and the maximum deviation occurs at full scale output. The advantage of a constant percentage error device for this application, as is the sine generator, is apparent when a series of multiplications is performed. The direction cosine matrix consists of a number of products of sine and cosine terms. The complete sine-cosine generator consists of the units shown in Fig. 7 (next page). The same type of network is used for the sine and cosine functions, the difference being that the sine generator is driven by a back-to-back sawtooth generator while the cosine generator is driven by an absolute value circuit.

There are several unique features incorporated in the equipment. For the purpose of studying missile systems involving two angles with continuous rotations, such as those encountered in the spinning or tumbling of a missile, two of the three sine-cosine generators have relay comparators that switch the polarity of the input angular rate and sine output whenever the angles exceed $\pm 180°$ (Fig. 8). These comparators have the advantages of minimizing the drift error normally associated with a rate resolver, as long as the operation remains within the range of $\pm 180°$, and the ability to sense both limits simultaneously. In other words, a missile could spin in one direction and then the other for a number of cycles, and the resolver would still be aware of the proper quadrant of operation. The operation of the sine-cosine generator for the second angle in the sequence is limited to less than $\pm 90°$. This angle generates the secant and tangent terms in the equations, and physically symbolizes gimbal lock in a gyro when it approaches $\pm 90°$. In the normal operation of the equipment, the scaling allows $\pm 65°$ variation of this angle without overloading. However, slightly improved accuracy can be obtained with the range relay for studies where the angle will not exceed $\pm 25°$. Note that for reasons of compatibility, the scaling of all angles is maintained in radians instead of degrees.

Whereas the normal scaling of the input angular rates was selected for maximum full scale rates of 1.0 radian per second per volt, *i.e.*, 100 P, 100 Q, and 100 R, the actuation of any of four rate scale relays will permit the following alternate input scales: 1000 P, 1000 Q, and 1000 R for maximum angular rates of 0.1 radian per second per volt; 300 P, 300 Q, and 300 R for maximum angular rates of $\frac{1}{3}$ radian per second per volt; 30 P, 30 Q, and 30 R for maximum angular rates of $3\frac{1}{3}$ radians per second per volt; and 10 P, 10 Q, and 10 R for maximum angular rates of 10 radians per second per volt. This feature permits ten to one changes in rate scale to either side of the normal.

A third feature in the computer allows three external Euler angles to be inserted in place of the computed Euler angles for situations where such angles already exist. This direct transformation relay is actuated from the patchboard.

The mechanization of the second increment of the Euler angle computer is shown in Fig. 9. This is a straightforward process of combining the proper terms of the direction cosine matrix with no scaling problems present. The mechanization of the third section is shown in Fig. 10. Three input velocities along the missile body axes (U, V, W) are transformed to the corresponding velocities in the ground reference frame ($\dot{X}$, $\dot{Y}$, $\dot{Z}$). Here again, since the direction cosine matrix represents unit vectors, the scaling of the output velocities is the same as the scale factor used with the input velocities.

A picture of the Euler Angle Computer is shown in Fig. 11. Fourteen dual electronic multipliers, eight quadruple amplifiers, three sine-cosine generator networks housed in an oven, and power supplies are contained in a four bay width structure. The fact that the computer is controlled through one connector means that the equipment can be completely checked out by disconnecting this one cable and hooking it to a special testing unit, where known combinations of inputs can be inserted and the outputs compared against predetermined values.

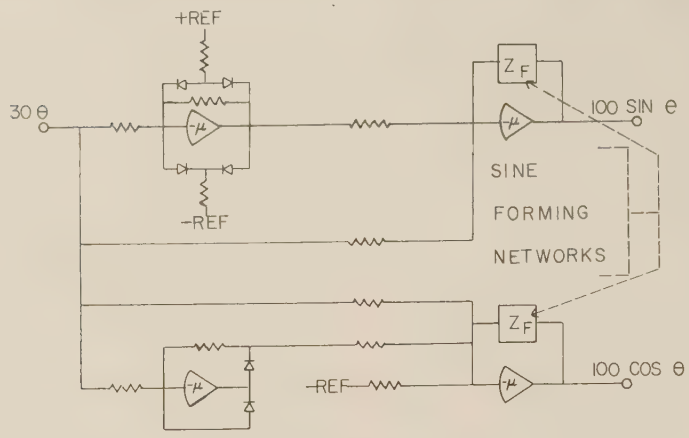

Fig. 7—Sine-cosine generator.

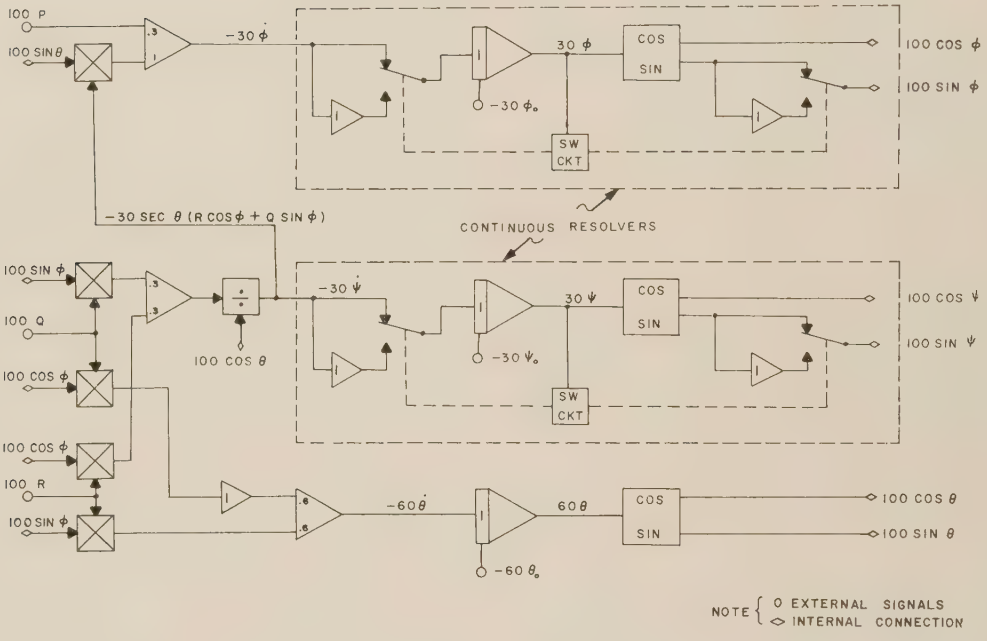

Fig. 8—Generation of Euler angles.

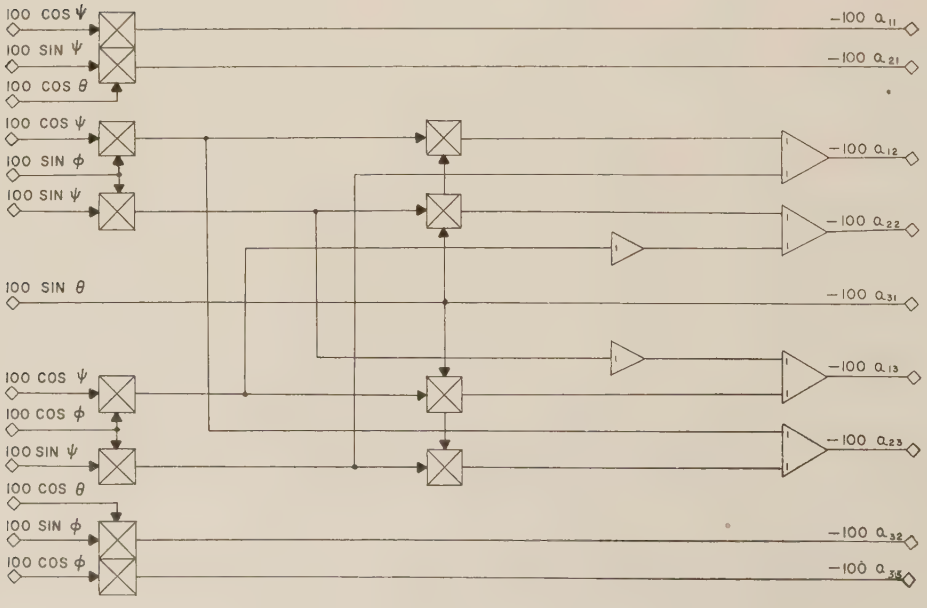

Fig. 9—Matrix generation.

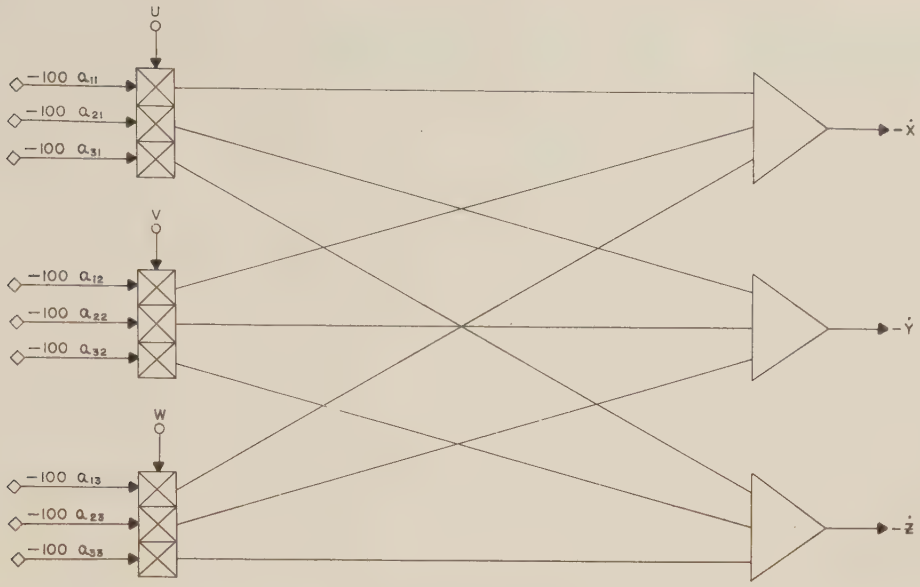

Fig. 10—Coordinate transformation.

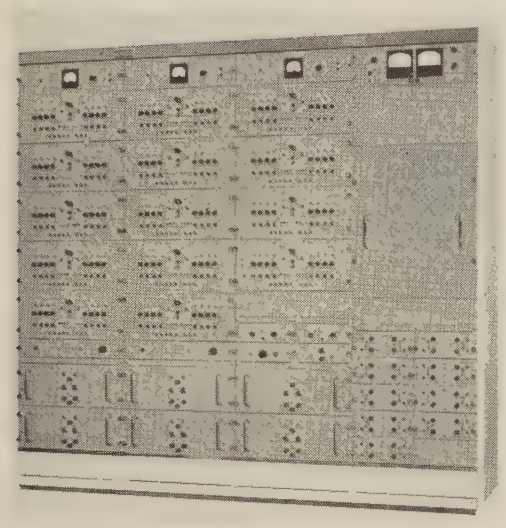

Fig. 11—Euler angle transformation computer.

The most important contribution by this computer to the simulation field is that the computer operator can now devote his full time to the problem of studying a missile system without worrying about the mechanization and trouble shooting of the coordinate transformation process. A more efficient and more accurate transformation is obtained, and a considerable saving in patchboard space results. The fact that all elements of the direction cosine matrix are brought out to the patchboard means that other transformations can be performed between the same two reference frames. For example, the gravity term in the ground reference frame is easily transformed into the missile rotating frame by multiplying three elements of the matrix by the proper constant.

IV. Conclusions

This Euler Angle Computer is a step towards increasing the effectiveness and usefulness of the analog computer. The reduction in setup time will more than pay for the machine within the period of a year. In the event that the requirements were to change, the type of components used would still be applicable to other types of solutions, merely by altering the wiring of the racks. This is not considered a possibility, though.

Other attempts to improve the accuracy and speed of the analog computer are being explored. The generation of arbitrary functions still remains the weakest link in analog simulation. Consideration is being given to the building of fixed function generators to be located in an oven assembly, similar to the one used in this Euler Angle Computer.

V. Acknowledgment

The author wishes to thank the personnel of the Flight Simulation Laboratory for contributing their efforts toward the completion of this paper, and especially J. Pappas, whose publication[4] provided the necessary mathematical background for this equipment.

Correspondence

The Neuristor*

A novel device and its properties have been hypothesized and possible digital systems employing it are briefly outlined in this note. The device, termed *Neuristor*, may be used to synthesize all digital logic functions, so that any digital logic system can be realized using arrays of neuristors only.

A neuristor may be visualized as a one-dimensional channel along which signals may flow. A signal propagates along the channel in the form of a discharge, followed by a "refractory" period, during which time a second discharge cannot be supported. The mode of discharge propagation is somewhat analogous to that which occurs along a "fuse," except that in the neuristor the channel exhibits perfect "healing." The refractory period can be thought of as the time of healing.

A discharge signal has the following properties: 1) attenuationless propagation, 2) uniform velocity of propagation, 3) a refractory period.

These characteristics are somewhat similar to the gross properties of transmission of discharge pulses by neurons in the nervous system—hence the name neuristor. A neuristor may be thought of as an electronic counterpart of the ionic neuron (in particular, the portion of the neuron that carries the propagating discharge).

In a sense, a neuristor may be considered to be a distributed version of a chain of suitably interconnected lumped-circuit monostable circuits. Devices of this type may be realized in many physical forms and may be based on many physical phenomena.

The basic requirements for the realization of such a device are: 1) a distributed energy source, 2) a distributed energy storage, 3) a distributed active device.

A distributed two-terminal active device is ideally suited to the realization of a neuristor; for example, a linear gas discharge structure; a length of bulk thermistor material; a length of four-layer diode; and so on. Let us consider a neuristor made of a strip of thermistor material (active device) connected in parallel with an equal length of distributed capacitor (energy storage), the parallel combination being fed, along its length, by a uniform distributed current (energy source). The distributed current source develops a uniform potential (V_0) along the channel which is below the magnitude of potential corresponding to the active region of the thermistor structure. In this condition the channel is stable. If the distributed capacity has a magnitude C per unit length, then in this equilibrium condition the channel is characterized by a "resting" energy of $\frac{1}{2}CV_0^2$ per unit length.

If any portion of the channel is suitably triggered (elevated to its active region), the energy stored at that portion is released into the channel with a corresponding increase of temperature of the local thermistor material. The increased temperature triggers the adjacent portions of channel, which in turn "fire," releasing their stored energy into the channel with a corresponding rise of local temperature, resulting in the subsequent firing of adjacent portions of the channel, and so on. In this manner, the discharge propagates at a uniform velocity and without attenuation. When the energy at any portion of the channel is discharged, that portion is "refractory" and cannot again be fired until its associated energy storage is suitably recharged. This process is characterized in Fig. 1(a), where a neuristor is indicated by a simple line drawing. The energy condition of the line (or channel) is shown at the instant of a passing discharge. For some distance behind the wavefront, the associated energy storage is in various states of discharge (portion labeled D). Behind this region the line is recovering, the associated energy storage being (re)charged from the distributed energy source. This portion is labeled C (for charge). The over-all length of the discharge and charge regions together represents the refractory distance R. A second discharge can follow immediately behind the refractory region, but not any closer, since there would then be insufficient energy to support this second discharge.

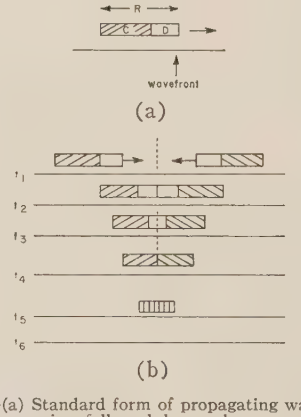

Fig. 1—(a) Standard form of propagating wave; discharge region followed by a charge region. (b) Collision of two discharges.

A very important consequence of the refractory period is that two discharge waves approaching each other on the same line disappear (annihilate each other) upon *collision*, since at the instant of collision there is zero (or low) energy on either side of the collision point and neither wave can "pass." This condition is indicated in the time sequence of Fig. 1(b).

Interconnection

A discharge along a line can be characterized by two variables, T and S, which measure, respectively, the magnitude of Trigger variable and (energy) Storage variable at any instant and at any position along the line. In the thermistor example of the previous section, T measures the local temperature and S the local stored capacitor energy. A propagating wave may then be characterized as indicated in Fig. 2(a).

A local increase in T causes a change in S (release of energy) which increases the local T of the adjacent section, resulting in a change of S, further down the line, and so on. T and S represent two components of the same wave, in a sense analogous to the case of linear propagation of electromagnetic waves, where a change with respect to time of E (electric field) generates H (magnetic field), and a change with respect to time of H generates E. T may be thought of as measuring the flow of trigger along the line, and S as measuring the flow of energy into (or transverse to) the line.

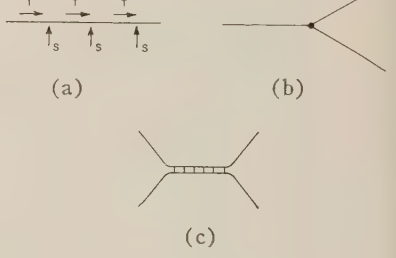

Fig. 2—(a) Relation of T and S variables in a propagating discharge. (b) T junction. (c) S junction.

Neuristors may be interconnected in two basically different modes, defined as T junctions and S junctions [Fig. 2(b) and 2(c)]. A T junction has the property that a discharge signal reaching it on any line triggers a discharge signal on every other connected line, each signal propagating away from the junction point with uniform velocity. T connected lines are coupled in their T variable. An S junction has the property that the refractory period following the passage of a wave on any one line is simultaneously experienced by all S connected lines; thus, all connected lines become mutually refractive as the result of the passage of a wave on any one of them. S connected lines are coupled in their S variable (but not their T variable). The connected lines share a common energy source, so that a propagating signal on any one line discharges the (common) energy, thereby making all channels mutually refractive (but without triggering discharge waves in the connected lines). A T junction (with three branches) is indicated by the heavy dot in Fig. 2(b). An S junction (between two channels) is indicated by the cross-hatching between the connected channels, Fig. 2(c).

* Received by the PGEC, April 29, 1960. The author, a staff member of Stanford Res. Inst. presently at Stanford University on leave of absence, is studying this technique as a Ph.D. dissertation program in the E.E. Dept. A more complete statement of these results is planned for publication. This work was supported under Contract NONR 225(31) NR 048 122, and Contract NONR 225(24) NR 373 360, jointly by the U. S. Army Signal Corps, U. S. Air Force, and U. S. Navy.

Logic

Before considering any simple logic arrangements, it is necessary to point out that two waves approaching each other on an S junction experience the same destructive collision process as two waves approaching on the same line. A moving "block" of D and C regions, symbolizing a propagating discharge, actually represents the state of local energy storage. As a block moves onto an S region, the block cannot be said to belong to either line, but rather to the pair of lines, since the state of energy is always identical for adjacent regions of S connected lines. Hence, the collision process takes the same form as that indicated in Fig. 1(b).

For the development of a logic system, consider first the storage of a binary variable. If a neuristor is close-looped, and is physically longer than one refractory length, then a pulse once started in the ring will circulate indefinitely (Fig. 3). Thus the value of a binary variable can be "stored" in a ring with the following representation: a pulse circulates in the ring to represent the value "1," no pulse circulates to represent the value "0." The state of the variable can be read via a T junction as indicated in Fig. 3. If the ring is circulating a pulse P, each time the pulse passes the junction it generates a pair of pulses P' and P''; the latter pulse continues the circulation and the former represents an output pulse. During each "revolution" of the pulse one output pulse is issued, so that the output line carries a uniform pulse train if the variable has the value "1" but remains unexcited for a variable value "0."

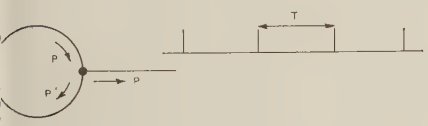

Fig. 3—Storage ring.

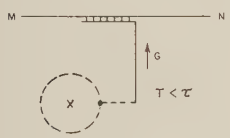

Fig. 4—Gate structure.

A basic gate structure is indicated in Fig. 4. The aim is to control the line MN by means of a gate signal G. Thus, with no gate signal applied, a pulse may be passed at will over the line MN. However, a single gate pulse G inhibits the use of the line for some interval of time. As long as the pulse G propagates along the S junction, no pulse may be passed from M to N since it would be sure to collide with G, resulting in the annihilation of both pulses. Define τ as the time of inhibition due to the pulse G. To inhibit the line MN permanently, it is only necessary to excite G from a pulse source whose pulse period T is less than τ. A storage ring may be used for this purpose, as indicated by the dashed structure in the figure so that if variable $x=1$ the line MN is permanently inhibited to use; if $x=0$ the line is completely free for use. The structure shown controls pulse propagation from M to N only, but symmetrical control can be obtained by use of a symmetrical gate. (Note that if $T>\tau$, and the attempt to pass a pulse along MN is unsynchronized with the pulse train controlling the gate, then a *probability* of pulse passage along MN is obtained.)

This gate structure represents an elementary example of the logic facility possible with interconnected neuristors. This structure is somewhat analogous to a relay coil and an associated contact. Actually, all digital logic functions may be realized in a simple manner by the extension of this approach.

Conclusion

Homogeneity seems to be the key characteristic of neuristor systems, and it is apparent on several levels.

A neuristor is a homogeneous device, a totally distributed active-passive structure providing both "device and wire" in one.

Logic networks are homogeneous because they may be derived with neuristors only. Conventional active "lumps," passively interconnected, do not exist.

Another aspect of homogeneity rests in the fact that information signals (pulses) throughout the system are everywhere describable in identical variables. There are no transducers; there is only one technology involved in the whole system.

Homogeneity occurs on still another level. An interesting property of the evolved logic systems is that any digital logic system, planar or not, may be physically realized in a two-dimensional plane. Neuristors need not cross in three dimensions, but may be made to connect in a plane while preserving noninteracting propagation properties. However, the use of such an arrangement requires that one line should not be used for some short (refractory) period after the other has been used; this is somewhat akin to the highway crossing problem, in which roads may be allowed to cross in a plane only if the system can be controlled so as to guarantee nonsimultaneous passage of vehicles (pulses). If this cannot be guaranteed then three-dimensional crossing structures in the form of "under- and over-passes" are required. It can be shown that any digital logic system can be realized in this manner, with guarantee of "safe," noninteracting pulse propagation at each such crossing structure. However, practical realization of such two-dimensional neuristor networks calls for (homogeneously) distributed logic and storage facility throughout the entire network.

Although no actual neuristors have as yet been constructed, there seems to be little question as to their physical realizability. In this light we should perhaps presently refer to these devices as "heuristors," reserving the name neuristor until they have become a *fait accompli!*

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Generalized RTL Circuits—Supplementary*

In a previous paper,[1] the author analyzed the tolerance margin and showed some typical applications of generalized RTL circuits, where quantized current levels are used to control the ON or OFF of a grounded-emitter switch, NOR circuit. It was demonstrated that a reliable multilevel NOR circuit can be designed with reasonably wide component and voltage tolerance, while the number of components, and hence the cost and space required, are much less than that for a straight digital approach.

In the analysis, approximations were made by assuming zero base-emitter and zero saturation voltage drop across the transistor junctions. Although this is applicable in many cases, it does tend to give optimistic answers, especially when the number of inputs increases. A supplementary analysis is presented here, taking into consideration the finite junction voltage drops of a transistor.

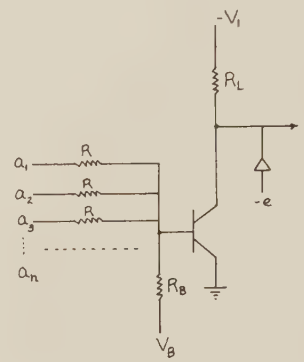

Fig. 1—Generalized NOR circuit.

Referring to Fig. 1, for a given type of p-n-p transistor, let:

- V_{bom} be the minimum base cutoff voltage required to insure safe operation
- $-V_{bsM}$ be the maximum negative base-emitter voltage drop when a transistor is switched ON
- $-V_{csM}$ be the maximum (negative) collector-emitter voltage drop (saturation drop) when a transistor is ON
- $-e$ be the output of an OFF NOR circuit corrected for clamping diode voltage drop, or corrected for loading when not clamped.

Cutoff Condition

For an m-level NOR circuit, the transistor stays cut off when $(m-1)$ of the n inputs, $a_1, a_2, \cdots, a_n$ are ON. We have

$$G_B(V_B - V_{bom}) \geq I_{co} + (V_{bom} + e)(m-1)G + (V_{bom} + V_{csM})(n-m+1)G.$$

* Received by the PGEC, June 20, 1960.

[1] S. C. Chao, "A generalized resistor-transistor logic circuit and some applications," IRE Trans. on Electronic Computers, vol. EC-8, pp. 8–12; March, 1959.

This simplifies to:

$$m(1 - a_{cs}) - I_B/I \leq 1 - I_{co}/I - a_{bo}(n + G_B/G) - a_{cs}(n + 1) \quad (1)$$

where

$$G = 1/R,\ G_B = 1/R_B,\ I = eG,\ I_B = V_B G_B,\ a_{cs} = V_{csM}/e \text{ and } a_{bo} = V_{bom}/e.$$

ON Condition

When m of the n inputs are ON, at $-e$ volts, the transistor is turned ON; and becomes saturated with collector current limited by external load resistance R_L. We have then

$$(e - V_{bsM})mG - (V_B + V_{bsM})G_B + (V_{csM} - V_{bsM})(n - m)G \geq I_L/\beta$$

where $I_L = V_1/R_L$. This simplifies to:

$$m(1 - a_{cs}) - I_B/I \geq I_L/\beta I + a_{bs}(n + G_B/G) - na_{cs} \quad (2)$$

where $a_{bs} = V_{bsM}/e$.

Define

$$k = 1 - a_{cs}$$

$$a_1 = 1 - (I_{co}/I) - a_{bo}(n + G_B/G) - a_{cs}(n + 1)$$

$$b_1 = (I_L/I\beta) + a_{bs}(n + G_B/G) - a_{cs}n.$$

Then (1) and (2) reduce to:

$$km - I_B/I \leq a_1 \quad (3)$$

$$km - I_B/I \geq b_1. \quad (4)$$

Fig. 2 shows a plot of (3) and (4), where the values of k, a_1 and b_1 are computed from the following data for purposes of illustration: $e=10$ volts, $V_{csM}=0.15$ volt, $V_{bsM}=0.30$ volt, $V_{bom}=0$ (typical MADT transistors show $V_{bom}=-0.1$ volt), $\beta \geq 50$, $I=1$ ma, $I_{co} \leq 0.05$ ma, $n=5$, $m=3$, $I_L=10$ ma and $G_B/G \sim 2.5$.

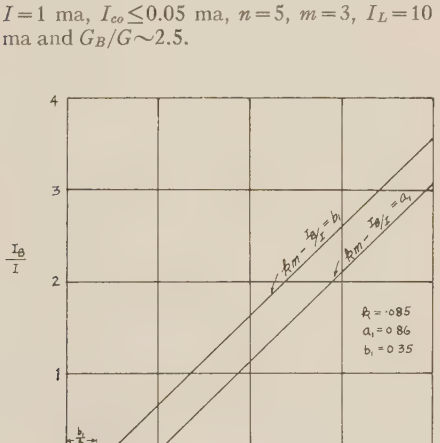

Fig. 2—Plot of (3) and (4), m vs I_B/I.

The allowable percentage tolerance, r, as defined in the referenced paper[1] is found from:

$$r = (a_1 - b_1)/[km - \tfrac{1}{2}(a_1 + b_1)]. \quad (5)$$

The critical condition is when $r=0$, *i.e.*, $a_1 = b_1$, which yields

$$1 - (I_{co} + I_L/\beta)/I = (a_{bo} + a_{bs})(n + G_B/G) + a_{cs}. \quad (6)$$

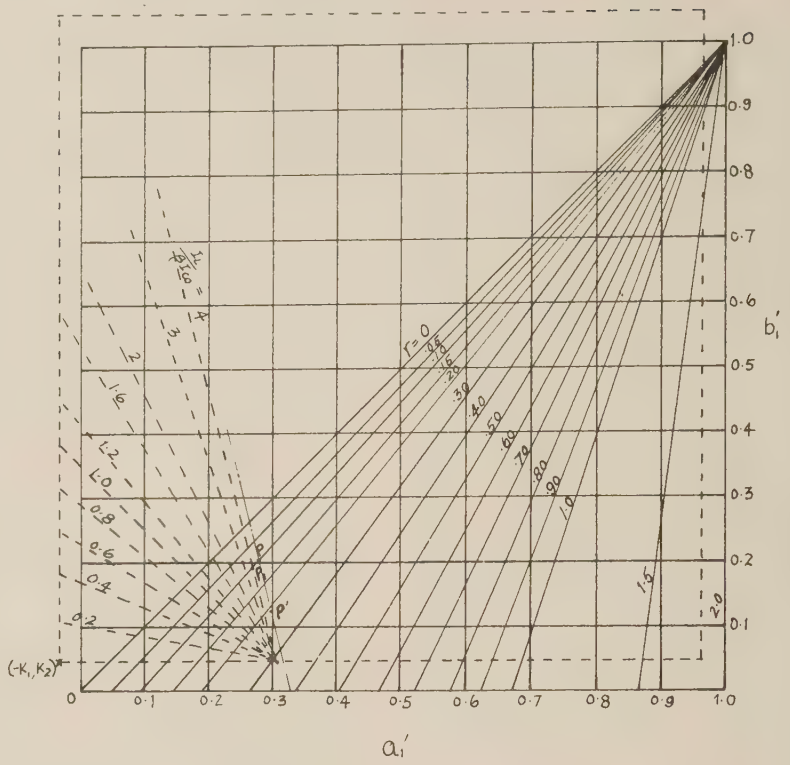

Fig. 3—Plot of (8) and (9) for $m=3$.

Eq. (6) can be used to estimate the upper limit of n, the theoretical maximum number of inputs, as shown in

$$(n)_{\max} \leq [1 - (I_{co} + I_L/\beta)/1 - a_{cs}]/[(a_{bs} + a_{bo})] - G_B/G. \quad (7)$$

Since $G_B/G = eI_B/V_B I \approx e(m - \frac{1}{2})/V_B$, (7) becomes

$$(n)_{\max} \approx [1 - (I_{co} + I_L/\beta)\, I - a_{sc}/[(a_{bs} + a_{bo})] - e(m - \tfrac{1}{2})/V_B. \quad (7')$$

For example, assuming $VB=10$ volts, and using the same set of parameters as in Fig. 2, $(n)_{\max}$ is approximately 22.

If a graphical solution is desirable, as shown in Fig. 3. of the referenced paper,[1] (5) may be converted to

$$r = (a_{1'} - b_{1'})/[1 - \tfrac{1}{2}(a_{1'} + b_{1'})] \quad (8)$$

where $a_{1'} = a_1/km$, and $b_{1'} = b_1/km$. Also, from the definition of a_1 and b_1, we have

$$a_{1'} + K_1 = 1/km - I_{co}\beta(b_{1'} - K_2)/I_L \quad (9)$$

where

$$K_1 = [a_{bo}(n + G_B/G) + a_{cs}(n + 1)]/km$$

$$K_2 = [a_{bs}(n + G_B/G) - na_{cs}]/km.$$

By shifting the origin to $(-K_1, K_2)$, (9) represents a set of straight lines passing through the point $(1/km, 0)$ on the new coordinates, and with a slope of $I_L/\beta I_{co}$. Using the same numerical example, $K_1=0.0305$ and $K_2=0.051$, a set of straight lines are obtained intersecting the new horizontal axis at $1/km=0.338$. For $I_L/\beta I_{co}=4$, if $r=0.10$ is desirable, a point P_1 is fixed which gives $a_{1'} \approx 0.275$ and $b_{1'} \approx 0.195$. Hence $a_1=0.812$ and $b_1=0.546$; and I and I_B are found to be 0.51 and 1.27 ma, respectively.

For comparison, when $a_{bs}=a_{cs}=0$, a point P is located which gives $a' \approx 0.28$ and $b' \approx 0.21$. Hence $a=0.84$, $b=0.63$, $I=0.32$, and $I_B=0.8$ ma. Alternatively, if the same $I=0.51$ ma is used, $a \approx 0.9$, $b \approx 0.4$, $a'=0.3$, and $b'=0.133$; a point P' is determined which gives $r=0.22$. This shows, as one would expect intuitively, that when considering the finite voltage drops across the transistor junctions, the margin of tolerance, r, is smaller than that obtained previously,[1] in which these junction voltage drops were assumed to be negligibly small. Thus, a larger input current and possibly higher beta transistors are required to maintain the same tolerance.

In order to speed up the graphical process, (9) may be plotted on separate tracing paper and overlaid on top of that of (8) (Fig. 3, solid-line part). Then the change of coordinates is just a matter of shifting the tracing paper around until the correct position is reached, the two sets of curves are then locked in position, and the rest of the design procedure is followed.

Measurements were made on many different types of transistors in order to arrive at some typical values of V_{bom}, V_{bsM} and V_{scM}. As many other workers have found, it was determined that MADT and Micro-alloy transistors are suitable for NOR circuit application. These transistors have typical junction voltage drops as given in the example.

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asting Out Threes in inary Numbers*

Rothstein[1] has described a method for termining the least non-negative residue odulo three of a number expressed in nary notation. This note describes a ethod for determining this residue which somewhat less intricate in its application, nd which appears more tractable to mechnization. As in Rothstein's method, actual vision by three is not necessary.

This method makes use of the congruence

$$N \equiv \sum_{i=0}^{n} a_i(-p)^i \text{Mod } (r+p),$$

here N is an integer expressed in the number system of radix r, a_i is the digit in the r^i rder of N, and p is an integer. The following roof of this congruence is an easy extension f the proof of the validity of the method of sting out nines in the decimal number ystem:[2]

$$N = a_n r^n + \cdots + a_1 r^1 + a_0 r^0 = \sum_{i=0}^{n} a_i r^i$$

$$= \sum_{i=0}^{n} a_i[-p + (r+p)]^i$$

$$= \sum_{i=0}^{n} \left[a_i \sum_{j=0}^{i} (-p)^{i-j}(r+p)^j C_j^i \right]$$

here

$$C_j^i = \frac{i!}{(i-j)!j!}.$$

aking the term corresponding to $j=0$ outide the interior summation:

$$N = \sum_{i=0}^{n} \left[a_i \left\{ (-p)^i + \sum_{j=1}^{i} (-p)^{i-j}(r+p)^j C_j^i \right\} \right].$$

since, in the interior summation, j now anges from one through i, each term of this ummation contains $(r+p)$ to some positive ntegral power; also, $(-p)^{i-j}C_j^i$ is an inger for all i and $j \leq i$. The interior summaion therefore can be replaced by $K_i(r+p)$,

K_i an integer. That is,

$$N = \sum_{i=0}^{n} a_i[(-p)^i + K_i(r+p)]$$

$$= \sum_{i=0}^{n} a_i(-p)^i + (r+p)\sum_{i=0}^{n} K_i, \quad \text{or}$$

$$N \equiv \sum_{i=0}^{n} a_i(-p)^i \text{Mod } (r+p).$$

* Received by the PGEC, June 13, 1960.

[1] J. Rothstein, "Résidues of binary numbers nodulo three," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, p. 229; June, 1959.

[2] See, for example, W. S. Humphrey, Jr., "Switching Circuits," McGraw-Hill Book Co., Inc., New York, N. Y., p. 78; 1958.

In the case at hand, $r=2$ and $p=1$.

$$N \equiv \sum_{i=0}^{n} a_i(-1)^i \text{Mod } 3$$

$$\equiv [a_0 \ominus a_1 \oplus a_2 \ominus \cdots \oplus (-1)^n a_n] \text{Mod } 3$$

This congruence is perhaps most easily applied as follows:

1) Obtain N_e, the modulo-three ring count of the ones in the even orders of N. (Even orders are those in which the radix 2 is raised to an even power.)
2) Obtain N_o, the modulo-three ring count of the ones in the odd orders.
3) Then $N \equiv (N_e - N_o) \text{Mod } 3$. If $(N_e - N_o)$ is non-negative, it is the least non-negative residue. If $(N_e - N_o)$ is negative, $3+(N_e - N_o)$ is the least non-negative residue.

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Digital Programming for the Inversion of *Z* Transforms*

In recent years, digital computer control has been a subject of considerable interest. The Z-transform technique has been widely used as a powerful tool. The analysis and design of digital and sampled-data control systems often necessitates the evaluation of inverse Z transforms. It has been shown in the literature[1] that inverse Z transforms may be evaluated by three methods: 1) from the real inversion formula by residue evaluation, 2) by partial-fraction expansion, and 3) by power-series expansion or long division. The third method is probably the simplest and the most convenient of the three. The evaluation may be performed with high accuracy in no time, provided that the inversion process is programmed on a high-speed digital computer. This note describes a digital program for the long-division inversion of Z transforms. With the aid of a high-speed digital computer, inverse Z transformation by this method is indeed a very simple task.

A Z-transform $G(z)$ containing q zeros and p poles can be expressed in the general form

$$G(z) = \frac{z^{-r}(a_r + a_{r+1}z^{-1} + \cdots + a_{r+q}z^{-q})}{1 + b_1z^{-1} + b_2z^{-2} + \cdots + b_pz^{-p}} \quad (1)$$

where $q+r=p$. In case $r=0$ and $q=p$, $G(z)$ may be written as

$$G(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2} + \cdots + a_pz^{-p}}{1 + b_1z^{-1} + b_2z^{-2} + \cdots + b_pz^{-p}}. \quad (2)$$

* Received by the PGEC, May 28, 1960.

[1] J. T. Tou, "Digital and Sampled-Data Control Systems," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 176–184; 1959.

In the above equations, the coefficients a's and b's are constants. Let the inverse transform of $G(z)$ be represented by the sequence

$$g^*(t) = g_0\delta(t) + g_1\delta(t-T) + g_2\delta(t-2T) + \cdots + g_k\delta(t-kT) + \cdots \quad (3)$$

where g_k denotes the value of $g^*(t)$ at the kth sampling instant and T is the sampling period.

Cross-multiplying (2) yields

$$(1 + b_1z^{-1} + b_2z^{-2} + \cdots + b_pz^{-p})G(z) = a_0 + a_1z^{-1} + a_2z^{-2} + \cdots + a_pz^{-p}. \quad (4)$$

Taking the inverse transform of the above equation term-by-term leads to a difference equation

$$g_n + b_1g_{n-1} + b_2g_{n-2} + \cdots + b_pg_{n-p} = a_0\delta_0 + a_1\delta_1 + a_2\delta_2 + \cdots + a_p\delta_p \quad (5)$$

where δ_0, δ_1, δ_2, $\cdots$ represent the sequence of a unit sampling function and they equal one at the respective sampling instants and zero otherwise.

From (5) it follows that for $n=0$, $g_0=a_0$; for $n=1$, $g_1=a_1-b_1g_0$; for $n=2$, $g_2=a_2-b_2g_0-b_1g_1$; and, in general, the value of $g^*(t)$ at the kth sampling instant is given by the recursion formula

$$g_k = a_k - \sum_{j=1}^{k} b_jg_{k-j}. \quad (6)$$

In the above equation, $a_k=0$ for $k>p$. Clearly, this recursion formula can readily be programmed on a digital computer.

When the Z-transform $G(z)$ contains more poles than zeros, $G(z)$ takes the form of the general expression given in (1). Cross-multiplying (1), one obtains

$$(1 + b_1z^{-1} + b_2z^{-2} + \cdots + b_pz^{-p})G(z) = a_rz^{-r} + a_{r+1}z^{-(r+1)} + \cdots + a_pz^{-p}. \quad (7)$$

Taking the inverse transform term-by-term yields

$$g_n + b_1g_{n-1} + b_2g_{n-2} + \cdots + b_pg_{n-p} = a_r\delta_r + a_{r+1}\delta_{r+1} + \cdots + a_p\delta_p. \quad (8)$$

Thus, it follows from the above equation that

$$g_0 = g_1 = g_2 = \cdots = g_{r-1} = 0 \quad (9)$$

for $n=r$, $g_r=a_r$, and for $n=r+1$, $g_{r+1}=a_{r+1}-b_1g_r$. In general, the value of $g^*(t)$ at the $(r+k)$th sampling instant is given the recursion formula

$$g_{r+k} = a_{r+k} - \sum_{j=1}^{k} b_jg_{r+k-j} \quad (10)$$

where $a_{r+k}=0$ for $r+k>p$. This recursion formula resembles (6) and can readily be programmed.

JULUS T. TOU
School of Elec. Engrg.
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Lafayette, Ind.

Contributors

David A. Aaronson (S'46–A'53) was born on November 20, 1921, in Victoria, British Columbia, Can., and there attended Victoria College. He received the B.Sc. degree from the University of Western Ontario, London, Ont., in 1949. He then studied at the University of British Columbia, Vancouver, where he received the M.A. degree in physics in 1950, and the Ph.D. degree in 1953.

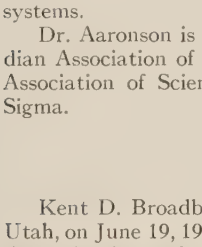
D. A. Aaronson

While a graduate student, he was associated with the Atomic Energy Division of the Canadian National Research Council, Chalk River, Ont., working on design and construction of a servocontrolled magnet current stabilizer. From 1953 to 1957, he was an engineering supervisor with Canadian Aviation Electronics, Ltd., Montreal, Quebec, engaged in design and development of an electronic flight and radar fire-control simulator. He was responsible for a training course for maintenance engineers for this equipment. He joined the technical staff of Bell Telephone Laboratories, Murray Hill, N. J., in 1957. His work there has been in research on high-speed electronics switching systems.

Dr. Aaronson is a member of the Canadian Association of Physicists, the Summit Association of Scientists, and Kappa Tau Sigma.

❖

Kent D. Broadbent was born in Provo, Utah, on June 19, 1926. He received the B.S. degree in physics from Brigham Young University, Provo, in 1949 and the M.S. degree in physics from Case Institute of Technology, Cleveland, Ohio, in 1951.



K. D. Broadbent

From 1951 to 1954, he was a Research Fellow at the University of Utah, Salt Lake City, engaged in nuclear reactor instrumentation studies. He joined Hughes Aircraft Company, Culver City, Calif., in 1954, to do research on advanced computer components; at the time of leaving, early in 1960, he was head of the Subsystems, Devices, and Components Section of the Information Processing Research Department, Hughes Research Laboratories. He is currently with American Systems Incorporated, Inglewood, Calif., where he heads a research effort into thin film devices and advanced information processing subsystems.

Mr. Broadbent is a member of Sigma Xi, Sigma Pi Sigma, and RESA.

M. Blythe Broughton (S'52–A'55-S'56–M'58) was born near Corbetton, Ontario, Can., on July 16, 1929. In 1954, he received the B.Sc. degree in radio physics and mathematics from the University of Western Ontario, London, Ont.

M. B. Broughton

For a year after graduation, he was an instrument design engineer for Orenda Engines, Ltd., a member Company of A. V. Roe (Canada) Ltd., in Malton, Ontario. He was employed by Computing Devices of Canada, Ltd., Ottawa, Ont., where he was a computer engineer until October, 1956, when he entered the University of Toronto as a graduate student. In 1958, he received the M.A.Sc. degree in electrical engineering. He was then employed as a systems engineer at the Canadian Armament Research and Development Establishment, Valcartier, Quebec, one of the research establishments of the Defence Research Board of Canada. He accepted his present post of assistant professor of electrical engineering at the Royal Military College of Canada, Kingston, Ont., in January, 1960.

❖

David T. Brown (S'58–M'60) was born in Milford, N. H., on April 11, 1936. He received the B.S.E.E. and M.S.E.E. degrees in 1959 from the Massachusetts Institute of Technology, Cambridge.

D. T. Brown

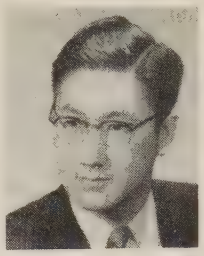
While at M.I.T. he was in the cooperative program of the Department of Electrical Engineering and was employed by the General Electric Company for three industrial assignments. In 1959 he joined the IBM Data Systems Division Product Development Laboratory, Poughkeepsie, N. Y., where he is concerned with improving digital computer reliability by coding for error control and introducing redundant circuitry to detect or correct faults in a machine.

Mr. Brown is a member of Eta Kappa Nu and Sigma Xi.

❖

Woo F. Chow (M'53–SM'53) was born in Shanghai, China, on June 7, 1923. He received the B.S.E.E. degree from Ta Taung University in 1945, and the M.S.E.E. and Ph.D. degrees in 1949 and 1952, respectively, from the University of Minnesota, Minneapolis.

He joined the Advanced Circuits Subsection of the Electronics Laboratory, General Electric Company, Syracuse, N. Y., in 1952. Since that time he has been engaged in research in high-frequency transistor circuitry and high speed digital circuits. In 1956, he became Project Engineer of various solid state circuit projects.

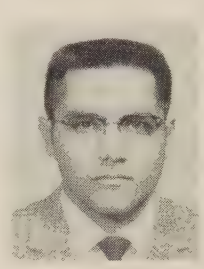


W. F. Chow

Dr. Chow is a member of Eta Kappa Nu and Sigma Xi.

❖

Gilbert R. Grado was born in El Paso, Tex., on October 25, 1926. He served with the U. S. Navy from 1944 to 1946 as an Aviation Electronic Technician's Mate. He received the B.S.E.E. degree from Texas Western College, El Paso, in May, 1949.



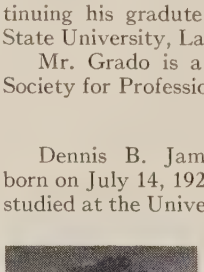
G. R. Grado

From 1950 to 1953, he was employed by the Diamond Ordnance Fuze Laboratory of the National Bureau of Standards in Washington, D. C., as a physicist, doing electronic circuitry research and development. In 1953 he joined the Instrumentation and Standards Branch of White Sands Missile Range, N. M., and since 1956, he has been associated with the Flight Simulation Laboratory at White Sands Missile Range. He has been head of the Engineering Maintenance Section during this time, as well as serving as a specialist in the Simulation Theory Branch this last year. He has taught servomechanisms, and analog computer courses at Texas Western College while continuing his gradute work at New Mexico State University, Las Cruces.

Mr. Grado is a member of the Texas Society for Professional Engineers.

❖

Dennis B. James (M'58–SM'60) was born on July 14, 1924, in Ruthin, Wales. He studied at the University of Wales, where he received the B.Sc. degree in 1948, and at Cambridge University of England, where he received the Ph.D. degree in 1953.



D. B. James

He was associated with the English Telecommunications Research Establishment from 1944 to 1946 and the Atomic En-

gy Research Establishment in Harwell, ngland, during 1946 and 1947. He was a search fellow at the University of British olumbia, Vancouver, from 1952 until 1954, hen he joined the technical staff of Bell elephone Laboratories, Murray Hill, N. J., here his first work was research on mag-tic core circuits. More recently he has been ncerned principally with electronic switch-g, including studies of time division switch-g circuits and pulse code modulation.

❖

D. B. Jarvis was born on February 8, 1937, in Cottinham, Yorkshire, England. e received his undergraduate degree in physics in 1958 from Birmingham University, England.

D. B. Jarvis

Since then, he has been employed at the Mullard Research Laboratories, Salfords, England, where he has studied various aspects of computing, particularly transistorized circuit logic.

❖

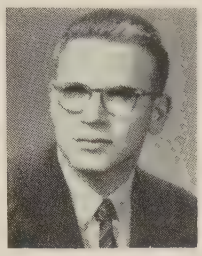
Robert L. Konigsberg (A'51–M'56) was born on May 23, 1921, in New York, N. Y. He received the B.E.E. degree in 1942 from Cooper Union Institute of Technology, the M.Ad.E. degree in 1948 from New York University, and the M.S.E. degree in 1954 from The Johns Hopkins University, Baltimore, Md.

R. L. Konigsberg

From 1942 to 1947, he was employed at the Western Electric Company, Kearny, N. J., as a test and standardization engineer in the Physical and Electrical Laboratory and as a product engineer in the Filter Department. In 1947, he joined the Fairchild Engine and Aircraft Corporation, Pilotless Plane Division, Farmingdale, L. I., N. Y., doing guided missile telemetering design and instrumentation work. In 1948, he was engaged in circuit design and development work on radar components for the DeMornay Budd Company in the Bronx, N. Y. From 1948 to 1951, he worked on guided missile telemetering design and instrumentation problems for the Glenn L. Martin Company, Baltimore. From 1951 to 1956, he was employed at the Radiation Laboratory of The Johns Hopkins University, doing research and development work in the electronics countermeasures field. Since 1956, he has been engaged in guided missile auto-pilot circuit design and development work at the Applied Physics Laboratory of The Johns Hopkins University, Silver Spring, Md.

Mr. Konigsberg is a member of Tau Beta Pi and Sigma Xi.

Eugene L. Lawler (M'59) was born in New York, N. Y., on July 28, 1933. He received the B.S. degree in mathematics from Florida State University, Tallahassee, in 1954 and the M.A. degree in mathematics from Harvard University, in 1957.



E. L. Lawler

He has worked for the National Bureau of Standards, Washington, D. C., and has done research in business data processing for Bay State Abrasives Corporation, Westboro, Mass. He has also worked as a teaching fellow at the Harvard Computation Laboratory. Presently he is working on methods for automatic computer design at Sylvania Electric Products, Inc., Needham, Mass., and studying at Harvard towards the Ph.D. degree in applied mathematics.

He is a member of the Association for Computing Machinery and Phi Beta Kappa.

❖

Richard Lindaman was born on April 7, 1926 in St. Paul, Minn. He received the Bachelor of Physics degree from the University of Minnesota, Minneapolis, in 1952.

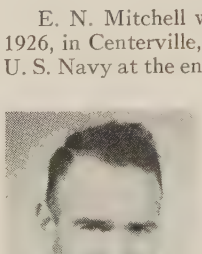
R. Lindaman

He spent several years in industrial chemical research including petroleum products, detergents, advanced battery development, and rheological studies. He also spent several years in technical publications work, writing instruction books on fire-control systems, missile launchers, and digital computers. In 1956 he joined Remington Rand Univac, a division of Sperry Rand Corporation, St. Paul, where he holds the title of physicist in the Mathematics and Logic Research Department. His major field of interest is formal logic, especially as applied to advanced digital computer design.

Mr. Lindaman is a senior member of the American Chemical Society.

❖

E. N. Mitchell was born on August 30, 1926, in Centerville, Iowa. He served in the U. S. Navy at the end of World War II as an electronic technician's mate. He received the B.A. and M.S. degrees in physics from the State University of Iowa, Iowa City, in 1949 and 1951, respectively, and the Ph.D. degree in physics from the University of Minnesota, Minneapolis, in 1955.



E. N. Mitchell

While at Iowa, he served as a teaching assistant in physics; and at Minnesota, he served as a teaching assistant during the academic year, and as a research assistant during the summer. From 1955 to 1958, he was employed in the Physics Department of Remington Rand UNIVAC, St. Paul, Minn., where he served as a research physicist and as supervisor of materials research. from 1958 to the present, he has been employed as an assistant professor of physics at the University of North Dakota, Grand Forks, where he is presently teaching and conducting research on the quasi-static properties of thin ferromagnetic films.

Dr. Mitchell is a member of Phi Eta Sigma, Phi Beta Kappa, Sigma Xi, and the American Physical Society.

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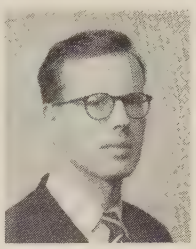
L. P. Morgan was born on January 5, 1931, in Purley, Surrey, England. He received the B.A. degree in physics in 1954 from Clare College, Cambridge University, England.

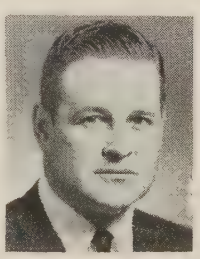


L. P. Morgan

Since then, he has been employed at the Mullard Research Laboratories, Salfords, England, working on many aspects of transistor circuit techniques, recently specializing in computer techniques. In January, 1960, he transferred to the Electronic Component Division and is presently in charge of the development of ferrite storage systems.

❖

Arthur V. Pohm (S'48–M'59) was born January 11, 1927 in Olmsted Falls, Ohio. After serving as an electronics technician in the U. S. Navy during World War II, he received the B.E.E. and B.E.S. degrees from Fenn College, Cleveland, Ohio, in 1950. In 1953 he received the M.S. degree and in 1954 the Ph.D. degree in physics, from what is now Iowa State University of Science and Technology, Ames.



A. V. Pohm

From 1950 to 1954 he was a research assistant with the Ames Laboratory of the U. S. Atomic Energy Commission and the Iowa State College Institute for Atomic Research. From 1954 to 1958 he held the following positions with Remington Rand Univac: research physicist, project physicist, and materials and applied physics research supervisor. Since December, 1958, he has been an associate professor of electrical engineering at Iowa State University of Science and Technology. At the present time he is conducting research on thin magnetic films and magnetic film devices under a National Science Foundation Grant.

Dr. Pohm is a member of Sigma Xi, Eta Kappa Nu, and Tau Beta Pi.

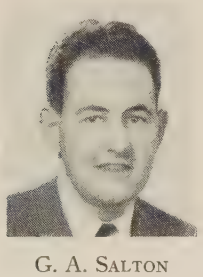
Alvin A. Read (S'48–A'50–M'54) was born on September 8, 1924 in Grinnell, Iowa. He received the B.S.E.E. and M.S.E.E. degrees in 1949 and 1952, respectively and the Ph.D. degree in electrical engineering in 1960, all from Iowa State College (now University), Ames.

A. A. READ

During World War II he served as an electronics technician in the Pacific. From 1949 to 1955 he was a research associate with the Ames Laboratory of the U. S. Atomic Energy Commission and the Iowa State College Institute for Atomic Research. Since 1955 he has been teaching and conducting research in the Electrical Engineering Department and the Engineering Experiment Station at Iowa State, where he is presently an associate professor. During the 1958–1959 academic year he was granted a Bendix Aviation Fellowship, followed in 1959–1960 by a National Science Foundation Science Faculty Fellowship. Currently he is engaged in the study of the application of thin ferromagnetic films in electronic devices. He is a co-author of several papers in this area.

Dr. Read is a member of Eta Kappa Nu, Phi Kappa Phi, Tau Beta Pi, Pi Mu Epsilon and Sigma Xi, and is a registered Professional Engineer in Iowa.

Gerard A. Salton (S'57–M'58) was born in Nuremberg, Germany, on March 8, 1927. He received the B.A. and the M.A. degrees in mathematics from Brooklyn College, N. Y., in 1950 and 1952, respectively.

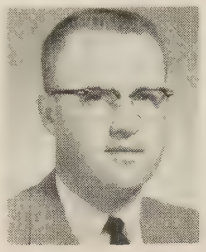


G. A. SALTON

Since 1952, he has been a staff member of the Harvard Computation Laboratory, Cambridge, Mass. In 1958 he received the Ph.D. degree in applied mathematics from Harvard University. Since 1958, he has been an instructor in applied mathematics at Harvard, teaching various computer courses. He has also been working on a part-time basis at Sylvania Electric Products, Inc., Needham, Mass., on Automatic computer design and other data processing problems.

Dr. Salton is a member of the Association for Computing Machinery, Sigma Xi, and Phi Beta Kappa.

Ralph F. Schauer (S'51–A'53–M'56) was born in Waterloo, Iowa, on May 31, 1930. He received the B.S. and M.S. degrees in 1952 and 1957, respectively, and the Ph.D. degree in electrical engineering in 1960, all from Iowa State University, Ames. During his Navy service from 1952 to 1955 he worked in naval communications and electronics. In the fall of 1955 he joined the academic staff of Iowa State University as an instructor in electrical engineering, and is now an assistant professor. He is also associated with the Cyclone Computer Laboratory, where he participated in the construction of an Illiac-type computer. He is now engaged in the modification program for the computer, as well as a research program in the system aspects of thin film devices.



R. F. SCHAUER

Dr. Schauer is a member of Eta Kappa Nu, Tau Beta Pi, Pi Mu Epsilon, Phi Kappa Phi, and Sigma Xi.

Robert M. Stewart, Jr. (M'49) was born in Washington, D. C., on May 6, 1924. He received the B.S.E.E. degree in 1945, and the Ph.D. degree in physics in 1954, both from Iowa State College, (now University), Ames.

R. M. STEWART

He taught in the Electrical Engineering Department of Iowa State College from 1946 to 1948. He then became a member of the Physics Department of Iowa State College where he taught and conducted research projects in the physics of the atmosphere. His major interest has been in specialized data acquisition and handling systems. He is presently responsible for the construction and operation of Cyclone, the Iowa State University digital computer. His present research activities are centered about the logical design of computer subsystems and computer logical components.

Dr. Stewart is a member of the American Physical Society, Phi Kappa Phi, Eta Kappa Nu, Pi Mu Epsilon, and Sigma Xi.

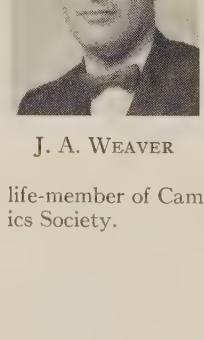
Robert M. Tillman (M'56) was born in Bessemer, Ala., on August 21, 1915. He obtained his formal electrical engineering background at the University of Alabama and at LaSalle College, Philadelphia, Pa.

R. M. TILLMAN

He served with the U. S. Navy from 1941–1945 as a Radio-Radar Officer in the American and Pacific Theatres, where he did laboratory development, prototype installation, and flight testing of new equipments. For ten years prior to joining Burroughs Corporation in 1955, he worked at the Naval Air Development Center, Johnsville, Pa., in the engineering design and flight testing of guided missile radio-telemetry systems. He is currently employed as a Staff Engineer in the Great Valley Laboratory of the Burroughs Research Center, Paoli, Pa., where he is engaged in the development of circuit and memory techniques for advanced airborne computers.

Mr. Tillman is a member of the Scientific Research Society of America, and holds a number of patents in his fields of interest.

J. A. Weaver was born on May 14, 1934, in North London, England. He received the B.A. degree in physics in 1957 from Trinity College, Cambridge University, England.



J. A. WEAVER

He has since been working at the Mullard Research Laboratories, Salfords, England, on several topics including precision angular measurement and high-speed computing techniques.

Mr. Weaver is a life-member of Cambridge University Physics Society.

Reviews of Books and Papers in the Computer Field

E. J. McCluskey, Jr., reviews editor, W. J. Cadden, asst. reviews editor

Please address your comments and suggestions to the Reviews Editor: Prof. E. J. McCluskey, Jr. Dept. of Elec. Engrg., Princeton University, Princeton, N. J.

A. Combinational Switching Circuit Theory and Boolean Algebra

The Decomposition of Switching Functions—R. L. Ashenhurst. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 29, pp. 74–116; 1959.)

This is a paper strewn with hidden gems; its results are presented, even buried, in refreshing understatement.

The paper is a fundamental study of the decomposability of switching functions into functions of functions where the variables for different levels are disjoint. An instance of simple decomposition

$$f(w, x, y, z) = F[x, y\phi, (w, z)]$$

$$f(w, x, y, z) = \bar{w}\bar{x}\bar{y}\bar{z} + \bar{w}xyz + wxy\bar{z} + w\bar{x}\bar{y}z$$

$$F(x, y, \phi) = \bar{x}\bar{y}\phi + xy\bar{\phi}$$

$$\phi(w, z) = \bar{w}\bar{z} + wz.$$

By generalizing the Harvard Chart to a "Decomposition Chart" the author shows how the necessary and sufficient conditions for the existence of such decompositions may be used to construct the composite function. This chart method appears feasible for up to six variables without the aid of a computer. Computer computation would seem to be quite lengthy to this reviewer.

Well-known factoring techniques of adding redundant terms to the function for simplification and then gating them out, is mentioned for making almost decomposable functions decomposable. The method had spotty usefulness for factoring, but perhaps is more powerful in this approach.

The only drawback to the paper is in the applications and examples. The applications seem to miss the significance of the method; the examples do not clarify it. This is especially apparent in the second part of the paper where nonsimple decompositions are considered in a fairly rigorous development of the general theory. This is excusable and perhaps even desirable, however, in pioneering work of such fundamental nature.

An instance of the most general form of disjunctive decomposition is:

$$f(A, B, C, D) = F[\theta[\phi(A), B], \varphi(C), D]$$

where A (etc.) stands for a set of variables disjoint with B, C, D. The structure of such complex decompositions is characterized in terms of simple ones and the nonuniqueness for associative composite functions developed.

In a series of theorems, Ashenhurst shows how complex decompositions may be constructed from simple ones detected from the decomposition chart. For example, if we have found the two simple decompositions:

$$f(A, B, C) = F[\varphi(A, B), C]$$

$$f(A, B, C) = G[\phi(A), B, C]$$

then we may construct the complex decomposition:

$$f(A, B, C) = F[\theta[\phi(A), B], C]; \qquad \theta[\phi(A), B] = \varphi(A, B).$$

These theorems represent a powerful extension for the use of the decompositions chart. Finally two theorems are proved which show how the existence of certain decompositions implies the existence of others. With this basis, Ashenhurst develops a general lattice structure of decompositions.

To grasp the import of these results for the practical designer requires the reader to write his own paper on the subject. The basic relationship of these results to practical (*i.e.*, economical) logical design is elusive, but one cannot help feel there are more hidden gems than meet the eye.

It should be realized that the result of decomposition is much like a generalized multilevel canonical form of the function. Each functional level may be minimized in itself but the over-all decomposition is devoid of any sense of minimality; it is expressed essentially in canonical terms. This is not to say it is not a tool for achieving minimality; its principal application, besides a basic understanding, is in this area. It should also be noted that this is not a solution of the factoring problem,[1] but probably of a very special case of it, namely for disjoint sets of variables.

Only one comparable work in scope and depth comes to the reviewer's mind; Post's "The Two-Valued Iterative Systems of Mathematical Logic."[2] The two have much in common.

In conclusion, this work perhaps needs done for it what McCluskey did for Quine.

John Earle
IBM Corp.
Poughkeepsie, N. Y.

[1] W. H. Burkhart, "Theorem minimizations," *Proc. Assoc. Comp. Mach. Meeting*, Pittsburgh, Pa., May 2–3, 1952; pp. 259–263.
[2] Princeton University Press, Princeton, N. J.; 1941.

The Use of Multipurpose Logical Devices—B. Dunham and J. H. North. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 30, pp. 192–200; 1959.)

In *The Computer and the Brain*, John von Neumann mentions the possibilities that "the individual neuron may be—at least in suitable special situations—a much more complicated mechanism than the dogmatic description in terms of stimulus-response, following the simple patterns of elementary logical operations, can express," and that "the nerve cell is activated by the stimulation of certain combinations of synapses on its body and not by others. . . . " Despite this and other conjectures that some neurons may function as logical operators of high order, little has been done to investigate the properties of polyadic relations (logical functions of n variables) beyond some general classifying and enumeration.

The present paper is a welcome exception, although its scope is confined to a special class of devices. As used herein, a "multipurpose" device is one that realizes certain n-adic relations, but these relations *per se* are not to be used. It is "adjusted" to produce a multiplicity of $(n-1)$-adic relations, and the adjusting technique discussed is that of biasing one of the inputs. For example, if one of the three inputs to a full binary adder is biased off and on, the "carry" output becomes the AND and OR functions respectively on the other two inputs.

Multipurpose devices are rated according to the number of different $(n-1)$ functions they can produce, and some tabulations of results are presented. Apparently all of the data were obtained by exhaustion procedures rather than by analysis; there is no contribution to underlying theory here, and this is certainly a direction in which more work can be done.

Douglas B. Netherwood
University of Michigan
Ann Arbor, Mich.

Simultaneous Logical Equations—Matrix Logic IV—E. J. Schubert. [(*Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 1080–1083; January, 1960.)]

This paper attempts to provide a solution to the following problem: In designing the instruction decoder for a digital computer, the

designer is assumed to know what the outputs of the decoder (gating functions) must be for each instruction which is to be decoded; the problem consists of choosing the n-bit binary operation codes for each instruction so as to minimize the decoder circuitry. The binary operation codes are the inputs to the decoder. The required gating functions are allowed to have "don't care" entries and are therefore regarded as ternary functions.

The author observes the fact that two or more gating functions may be merged (*i.e.*, replaced by a single function) provided such functions assume no contradictory values for any instruction which is to be decoded. He then proceeds to perform such mergers in a completely arbitrary order. When no more mergers are possible, he chooses from the merged set of gating functions n members "having the highest entropy," *i.e.*, those n functions in which the numbers of 1's and 0's are as nearly equal as possible. These n functions are then identified with the inputs to the decoder (*i.e.*, the n bits of the operation codes), and the remaining gating functions are expressed as Boolean functions in terms of these inputs.

The paper suffers from several grave deficiencies. First of all, some of the premises are rather questionable. For instance, Theorem III appears to be a definition of somewhat questionable merit rather than a true theorem, since it implies that the complexity of a circuit which realizes a given Boolean function depends solely on the number of minterms either included in, or excluded from the function, whichever is less; (for a function of p variables, there are 2^p possible minterms which either are or are not included in the function). This assumption seems shaky since it is quite easy to construct two functions (each a function of n variables and each containing less than 2^{n-1} minterms) such that the function with fewer minterms results in the more complex circuit. One may also observe that since the order in which the gating functions are merged is perfectly arbitrary, and since widely different mergers may result depending on that order, then it is not unlikely that the economy of the final code may be quite poor if an unfortunate order of merging is chosen. The last sentence of the paper shows that the author is aware of this problem.

The author uses a matrix notation which he developed in previous papers.[1,2] It is this reviewer's feeling that this notation does not simplify any of the steps which have to be performed in solving a problem of the type treated in this paper, and that the use of this notation here is therefore questionable. Furthermore, the author is very inconsistent in his use of symbols. The following four statements appear within four consecutive paragraphs in the first section of the paper (underlining is by reviewer):

1) " . . . the binary output Y_z by the dot product of coefficients F_{zi} and N_i."
2) "Propositions Y_z may be defined with respect to the constraints Z_k by a matrix of coefficients C_{zk}."
3) " . . . the outputs Z_k with respect to the inputs Y_z."
4) " . . . satisfy the propositions Y_z in such a way that all constraints C_{zk} are met."

The following typographical errors have been noticed:

1) In the illustrative example, which the author borrows from a paper by E. Hirschhorn,[3] the *inputs* (*operations*) Y_z and the *outputs* (*gating functions*) Z_k of the decoding network are interchanged, so that the particular problem solved by the author is entirely different from the one proposed by Hirschhorn.
2) Definition of identify (3D), first line, should read:

$$A \equiv B \quad 0\ 1\ 2.$$

3) Eq. (5B), first line, should read:

$$\frac{dH}{dp} = 0 = \log p - \log (1 - p).$$

4) Third line above (11) should read:
"If a bit or column k comprises at least t irrelevant entries 2, . . . "

[1] E. J. Schubert, "Matrix analysis of logical networks," *Commun. and Electronics*, No. 35 (*Trans. AIEE*, pt. I, vol. 77), pp. 10–12; March, 1958. (Review in the IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, p. 505, December, 1959; by E. J. McCluskey, Jr.)
[2] E. J. Schubert, "Matrix synthesis of high speed logic," *Commun. and Electronics*, No. 41 (*Trans. AIEE*, pt. I, vol. 78), pp. 4–8; March, 1959.
[3] E. Hirschhorn, "Simplification of a class of Boolean functions," *J. Assoc. Comp. Mach.*, vol. 5, pp. 66–75; January, 1958.

Because of the above difficulties with both the substance an form of this paper, the contribution made by this article appears, a least to this reviewer, to be somewhat problematic.

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The Application of Graph Theory to the Synthesis of Contact Net works—R. Gould. (*Proc. Internatl. Symp. on the Theory of Switching* April 2–5, 1957, in "Annals of Computation Laboratory," Harvar University, Cambridge, Mass., vol. 30, pp. 244–292; 1959.)

This is the main part of the author's doctoral thesis at Harvar University, 1957, and it describes a general matrix-algebraic metho of realizing contact 2-terminal networks for any Boolean functior The networks obtained are minimal in many and possibly in all case (p. 272). He removed the hitherto existed limitation of the singlenes or noniteration of contacts in this method. The paper deserves specia attention from network researchers because this forms the first ex ample of the algebraic topological "connection synthesis." In othe words, now it has become possible to find any ingenious connectio by algebraic routine work, and this idea of adopting the loop or cut set matrix as unknown quantity is principally extensible to any othe network synthesis. Actually he had succeeded in finding many ne networks with less contacts than any previously known solutions i the case of four Boolean variables.[1] For realizing a graph from it loop matrix, a new general method[2–4] is used. The cut-sets are alge braically expressed by cut-set vectors. This cut-set approach will lea to the establishment of a dual synthesis of Boolean functions.[3,5]

The prime implicant and other expressions of the given functio are expressed in the loop matrix M modulo 2, and by the well-know Jordan's diagonalization process, linearly dependent loop vectors ar eliminated; and then all possible loops passing the relay and sourc are determined by the linear combination of the remained independ ent loop vector set L. If these are either included in the origina Boolean function or if they contain at least one pair of make an break contacts of one relay which is called a "blocked loop" o "pseudotie," then L is called "acceptable" and realized as a graph Some L become realizable by the addition of adequate blocked loops. If L is not realizable, the number of contacts is increased an the similar process is repeated until the graphs are obtained.

If combinatorial analysis, various topological enumerations fo loop and cut-set matrices and some abstract algebraic concepts ar fully applied, this conventional method for manual computation wil be developed to a rigorous method of general switching networ synthesis for which the use of computer becomes possible.

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[1] R. Gould, "A note on contact networks for switching functions of four varia bles," IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-7, pp. 196–198; September 1958.
[2] R. Gould, "Graphs and vector spaces," *J. Math. Phys.*, vol. 37, pp. 193–214 October, 1958. Its dual, that is, realization of graphs from its cut-set matrix is published in Okada *et al.*,[3] and Mayeda.[4]
[3] S. Okada, Y. Moriwaki and K. P. Young, "Realization of Boolean polynomials based on incidence matrices," *Proc. EJCC*, Boston, Mass., pp. 120–132; December 1959. Also see Microwave Res. Inst. Res. Rept. R-790-59, Polytech. Inst. o Brooklyn, Brooklyn, N. Y.; November, 1959.
[4] W. Mayeda, "Necessary and sufficient conditions for realizability of cut-set matrices," IRE TRANS. ON CIRCUIT THEORY, vol. CT-7, pp. 79–81; March, 1960.
[5] C. Saltzer, "Algebraic topological methods for contact networks analysis and synthesis," *Quart. Appl. Math.*, vol. 17, pp. 173–183; July, 1959.

Matrix Methods in the Theory of Switching—Warren Semon. (*Proc Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 30, pp. 13–50; 1959.)

This paper was written as an introduction to the subject of Boolean matrices. As the title indicates it is of primary value to those concerned with switching theoretic problems; providing both an introduction to the use of matrix methods, as well as some interesting new ideas.

The use of simultaneous Boolean equations in minimization theory is most instructive, and represents an intriguing approach which can undoubtedly be adapted to machine computation. Here for example, the evaluation of $2m(n+1)$ coefficients will suffice to find all circuits of a given form with m branches and n variables

ch will satisfy a given function. Since one can start with a simple uit form and gradually try more complicated structures until a ution is reached with only one contact per branch, the first solu- s obtained will be minimum as long as the structures are intelli- tly chosen. This represents a significant advance, since standard niques have usually involved enumeration of a large number of r minimal circuits before one can have reasonable certainty of ing obtained a minimum circuit.

Some minor oversights make the paper a little confusing on first ling. For example, the letter n is used on three consecutive pages stand respectively for the number of terminals in a circuit, a rix subscript, and the number of variables in a function. It is also imes not completely clear what the restrictions are on the various orems. Theorems 9 and 11, for example, imply some restrictions he terminals used for outputs, and theorem 12 is not clear without efinition of a triangularized Boolean matrix.

It is unfortunate that a slightly more comprehensive treatment not given of matrix circuit design techniques, for then the earlier tions could have well served the dual purpose of introducing the ject to both the engineer and mathematician.

In summary, the paper is worth reading, in spite of its minor wbacks. The generally clear presentation together with the many npletely worked out examples provide the studious reader with ple material for detailed study.

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a Theory of Boolean Functions—S. B. Akers, Jr. (*J. Soc. Indus. pl. Math*, vol. 7; December, 1959.)

The concept of *Boolean difference* is introduced and its elementary perties are derived, after which a functional, called the *Δ-operator*, efined in terms of the Boolean difference. These concepts are used a basis for developing some formal relationships in Boolean alge- .

For example, they are used to obtain the Reed-Muller expansion, d in fact, a more general formulation is derived:

$$F(x_1, \cdots, x_m, y_1, \cdots, y_n) = a_1{}^0 \oplus a_1{}^1 x_1 \oplus \cdots \oplus a_m{}^1 x_m \oplus \cdots \oplus a_1{}^m x_1 \cdots x_m.$$

In this equation the symbol $\oplus$ means "exclusive or," and the efficients $a_i{}^j$ are Boolean functions of $y_1, \cdots, y_n$. They are, in t, evaluated explicitly as Boolean differences of orders 0 through the order specified by the superscript.

Necessary and sufficient conditions are derived for functional de- ndence, functional decomposition, and the solution of Boolean uations.

The author's primary object is to provide a theory unifying exist- knowledge. Consistent with this, some of the theorems stated are mply paraphrases into the difference terminology of primarily own theorems. However, some new ground is broken, and the derlying fundamental connection between different results by dif- ent authors is brought out. The indicated analogies, *e.g.*, between olean differences and finite differences, between functional de- pendence in Boolean algebra and functional dependence in the eory of continuous functions, are not developed to their fullest vantage; and in this respect there might be a considerable ad- ntage to choosing a notation that capitalized more fully on such alogies.

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e Shortest Path Through a Maze—Edward F. Moore. (*Proc. ternatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The nals of the Computation Laboratory," Harvard University, Cam- dge, Mass., vol. 30, pp. 285–292; 1959.)

This paper provides several algorithms for finding the shortest ute on a linear network from a given origin to a given destination. sentially the same methods have been used by several other authors[1–4] (which does not exhaust the literature on this problem). However, each of these authors has a bias towards either a particular setting for the problem, a special method of proof, or a personal criterion for an optimal algorithm. The emphasis in the present version is on considerations of memory capacity and the implications of synchronous or asynchronous circuit operation for the proposed algorithms.

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[1] L. R. Ford, Jr., "Network flow theory," RAND Paper P-923, 1956.
[2] G. B. Dantzig, "Discrete variable extreme problems," *JORSA*, vol. 5, pp. 266–277; 1957.
[3] R. Bellman, "On a routing problem," *Quart. Appl. Math.*, vol. 16, pp. 87–90; 1958.
[4] G. B. Dantzig, "On the shortest route through a network," *Management Sci.*, vol. 6, pp. 187–190; 1960.

Symmetric Polynomials in Boolean Algebras—S. Seshu and F. E. Hohn. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 30, pp. 225–234; 1959.)

This paper, written from the point of view of a pure mathematician, rather than an engineer or a logician, is based on Stone's classical paper, "Representations of Boolean Algebras."[1] The primitive operations (called addition and multiplication and symbolized by "$+$" and juxtaposition) in a Boolean ring normally correspond to *symmetric difference* in the calculus of sets or *exclusive or* in the propositional calculus, and to *intersection* (meet) in the calculus of sets or *conjunction* in the propositional calculus, respectively; the dual interpretation is possible. A Boolean ring is a multiplicatively idempotent, necessarily commutative, ring. The authors go on to require a unit (multiplicative identity) although Stone (Definition 1) does not require this; he does show that finite Boolean rings always have a unit. Following Stone, a new operation is defined by $a+b+ab$, and symbolized by "$\vee$." This operation normally corresponds to *union* (join) in the calculus of sets or to *disjunction* (inclusive or) in the propositional calculus. As is well known, if a Boolean ring does have a unit, say e, and we define the complement of a as $a+e$, then complement, "$\vee$," and ring multiplication, satisfy (and indeed in two ways) all the axioms for a Boolean algebra. Boolean (-algebraic) functions are defined as those corresponding to well-formed expressions containing variables and $\vee$, multiplication, and complement. The authors state that the set of all Boolean functions with arguments ranging over a Boolean algebra, B (actually all with the *same number of variables*) form a Boolean algebra. It is also the case that all Boolean-ring functions (corresponding to well-formed expressions containing variables and $+$, multiplication) of n variables form a Boolean ring.

The reviewer enthusiastically applauds the notational trend initiated by Stone in 1936 and here continued by the authors. It has been all too common in the engineering literature to use a plus sign for *or* and to use the symbol "$\oplus$" to represent what is here represented by "$+$." Since the latter corresponds to binary addition without carries and always has an inverse, it is much closer to ordinary addition than an operation that yields the result: $1+1=1$. The reviewer would like to suggest the following preferred symbols: In abstract Boolean algebras and lattices; $\bigvee$, $\bigwedge$, for least upper and greatest lower bounds, respectively. The down wedge is pushing down from above, and the up wedge is pushing up from below. For the calculus of sets; $\bigcup$, $\bigcap$, for union and intersection, respectively. For the propositional calculus; $\vee$, & (or mere juxtaposition) for disjunction and conjunction, respectively.

The atoms of the induced Boolean algebra (minterms in the engineering terminology) are introduced and named *fundamental products*. The fact that these form an atomic basis is, curiously enough, not mentioned. Nontrivial Boolean rings are richly supplied with divisors of zero, and if $ab=0$, the authors call a and b orthogonal (but mark you, there is no inner product). If a and b are orthogonal, $a \vee b = a+b$.

Distinct atoms are thus orthogonal, and the *distinguished* disjunctive normal form can also be written as a ring expansion with every "$\vee$" becoming a "$+$." The occurrences of complements can be

[1] M. H. Stone, "Representations of Boolean algebras," *Trans. Am. Math. Soc.*, vol. 40, pp. 37–111; 1936.

eliminated by introducing constants, since $a=a+1$, leading to a canonical form that is a sum of symmetric products

$$\sum_{i=0}^{2^n-1} \phi_i \prod_{j=1}^{i} x_j$$

where the ϕ_i are constants, *i.e.*, elements of the underlying Boolean ring. The set of Boolean-ring functions of n variables is a module (Jacobson's and Bourbaki's terminology[2,3]—the authors call it a vector space) over the Boolean ring.

The remainder of the paper studies in detail the properties of symmetric polynomials over B. It is shown that the set of symmetric polynomials is also a Boolean (sub) ring, and indeed a submodule of dimension $n+1$ over B with a basis consisting of the fundamental symmetric functions, defined in the paper, and which constitutes an orthogonal (see above) basis.

The set of symmetric functions in n literals (variables and complements thereof), is also studied with the aid of input-transformation (variable-complementing) matrices, and shown to have a somewhat more complicated structure.

The paper is not restricted to a 2-element Boolean algebra of scalars and the authors point out this increase in generality. Unless the number of signal states is a power of 2, it would seem that Post algebras may be more useful in the applications.

Although the results in the paper are of theoretical interest, especially in the theory of modules, and a commendable step in the direction of properly identifying "switching algebra" with its mathematical bases, the reader will look in vain for any applications to switching circuits.

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[2] N. Jacobson, "Lectures in Abstract Algebra," "Linear Algebra," D. Van Nostrand Co., Inc., Princeton, N. J., vol. II, p. 7; 1953.
[3] N. Bourbaki, "Elements de Mathématique," vol. II, Algèbre, Hermann & Cie., Paris, France; Chapt. 2.

B. Sequential Switching Circuit Theory and Iterative Circuits

Remarks on the Design of Sequential Circuits—M. Rubinoff. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 30, pp. 241–280; 1959.)

The design of sequential circuits is discussed by means of "command graphs" and "dispatcher tables." The command graph is similar to a state (transition) diagram, except that the nodes are labeled in terms of the present state and the input responsible for the present state. Directed branches indicate allowed transitions between nodes. The dispatcher table, derived from the command graph, is essentially the Huffman flow table in rearranged form. The dispatcher table is used for secondary assignment, and eventually for circuit design.

The author's primary claim for the command graph is that it assists the designer in the initial conversion of the verbal problem statement to a tabular form suitable for detailed examination of hazards and for state assignment. The validity of this claim is debatable; most designers, with even limited experience, can probably construct a flow table directly from the problem statement. Further, since a single state may appear in several nodes on the command graph, the connectivity of the machine cannot be obtained at a glance, but must be determined from the dispatcher table by using matrix methods, as described in the paper.

The paper is well organized and carefully written, and contains several examples taken from previous literature. The style is that of the instructor, who conveys ideas by example and exhortation rather than by rules and proofs. Rubinoff's nomenclature is somewhat different, and perhaps more descriptive, than that of his predecessors. There is a thorough discussion of the various hazards encountered in sequential machines due to nonsimultaneous events, metastable conditions, and delays. Although this discussion is not new, it is presented with sufficient clarity to be valuable from a tutorial point of view.

If this paper were to form part of a text book on switching circuit design, it would be considered as a thorough presentation of the design problem. Since the text books available in 1957 did not as yet make use of the "state" concept, Rubinoff's work is commendal because it brought together and presented clearly the ideas of predecessors.

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A Comparison of Sequential and Iterative Circuits—E. J. McCluske Jr. [(*Trans. AIEE, Commun. and Electronics*, No. 46 (*Trans. AIE* pt. I, vol. 78), pp. 1039–1044; January, 1960.)]

The author illustrates, by way of an example, the design of iterative network. The method described is that of designing firs sequential network to perform the desired operation serially. T sequential circuit is then modified slightly, and repeatedly redra to form an iterative network that will perform the desired operati in a parallel mode.

Dr. McCluskey then proceeds to a discussion of iterative circui The discussion is generally limited to iterative networks with one o put line for the entire network, although one example with two o puts is shown.

Although interesting, this paper appears to have only limited u and leaves many questions unanswered. The coding problem e countered in sequential network theory now displays itself as a codi problem concerned with connecting iterative cells. Associating t two problems adds to our understanding, but does not solve eit problem.

Unfortunately, an error in the reading of the Karnaugh map Fig. 5(b) leads to errors in Figs. 5(c) and 6.

This paper appears to be rather brief to cover the large subj proposed and the reviewer would be interested in further extension the subject.

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An Algebra for Periodically Time-Varying Linear Binary Sequen Transducers—D. A. Huffman. (*Proc. Internatl. Symp. on the Theo of Switching*, April 2–5, 1957, in "The Annals of the Computati Laboratory," Harvard University, Cambridge, Mass., vol. 30, p 189–203; 1959.)

The analysis of linear systems can be pursued in many languag Conventional time invariant linear systems lead to transfer functio which are ratios of polynomials in the Laplace variable, s, with co ficients from the real number field. Taking an inverse transform such a transfer function leads to a time function defined on a contin ous time interval—the impulse response of the linear system. O sampled data colleagues consider linear systems with inputs a outputs defined only at discrete time instants. By noting that su systems have transfer functions containing s only in the form e^{sT} th introduce the variable $z=e^{sT}$ and the Z-transform. The transf functions so derived are the ratios of polynomials in z with coefficien from the real number field. Taking an inverse transform of such transfer function leads to a time function defined on a set of discre time instants—the impulse response of the sampled data linear sy tem.

For yet another class of problems[1] it is desirable to restrict t inputs and outputs of a sampled data linear system to be elements a smaller field (or ring). Such a system with binary inputs and ou puts is what Huffman has termed a linear binary sequence tran ducer. These linear systems have transfer functions which may thought of as ratios of polynomials in z with the coefficients tak from the number field containing only 0 and 1. In previous papers Huffman has pointed out the advantages of viewing linear bina sequence transducers in terms of such transfer functions, and h defined z (or z^{-1}, depending on your dialect) as the delay operator Taking an inverse transform of Huffman's transfer function (no the ratio of polynomials in D) leads to a sequence of binary numbe —the impulse response of the binary sampled data linear system.

In this paper Huffman extends the idea of such transfer functio to include the case of periodically time-varying linear binary s

[1] Juris Hartmanis, "Linear multivalued sequential coding networks," IR Trans. on Circuit Theory, vol. CT-6, pp. 69–74; March, 1959.
[2] D. A. Huffman, "The Synthesis of Linear Sequential Coding Network *Trans. of the Third London Symp. on Information Theory*, Butterworth, Londo pp. 77–95.
[3] D. A. Huffman, "A linear circuit viewpoint on error correcting codes," IR Trans. on Information Theory, vol. IT-2, pp. 20–28; 1956.

ence transducers. The transfer function of such a linear system is ain the ratio of polynomials in D, but now the coefficients of the ynomial are periodic binary functions of time—a result analogous results in time-varying conventional and sampled data linear sys- ns. The properties of these networks are discussed in some detail. e property worth mentioning (it also holds for other types of iodically time-varying linear systems) is that two such networks y be cascaded, but they do not necessarily commute.

The synthesis of these transducers is described in terms of a mmutator" element which provides the time-varying properties ich Huffman needs. These commutator elements lead to a par- ularly neat and concise method of representing the system in block gram form and of relating the block diagram to the transfer ction.

As usual, Huffman presents a lucid discussion of an interesting cept and develops it to the point where the reader can see exten- ns and applications of the paper. For example, the systems de- ibed seem to be ideally suited to the instrumentation of cyclic ary group codes.

There is a typographical error in (1.6) of this paper. It is left as exercise for the reader.

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C. Pattern Recognition and Learning Theory

On the Mechanical Simulation of Habit-Forming and Learning — ul Gorn. (*Information and Control*, vol. 2, pp. 226–259; 1959.)

Two Notes on Machine Learning—Henrik H. Martens. (*Informa- n and Control*, vol. 2, pp. 364–379; 1959.)

Despite the apparent similarity of their titles, these papers of rn and Martens treat entirely dissimilar subject matter. On one nd, Gorn is concerned with the use of computers as a tool for the dy of animal behavior. Martens, on the other hand, emphasizes e point that his object is "to study a form of machine behavior be- ved to be of interest in its own right; (he makes) no attempt to set models for human or animal brain functions."

Gorn's paper considers in great detail the technique of represent- stochastic models of animal learning and habit-forming by en- mbles of computer subroutines. Although behavioral scientists ve been simulating such models on computers for some time (the t-rats of Bush and Mosteller, for example), Gorn's approach is ite different from that of a psychologist making use of Monte rlo methods to test a particular theory. Instead, the system to be nulated is analyzed into its component functions, each of which is nsidered independently. The paper specifies a computer realization the functions of random selection and reinforcement for a number models of current interest. Although the extensive formal treat- ent applied to some of these models will appeal principally to those ll-steeped in the subject matter of mathematical learning and de- ion theory, Gorn's paper can be profitably read by psychologists o are yet unaware of the great versatility of the computer as an strument for the study of animal behavior.

This reviewer must take exception, however, to a statement ich, while irrelevant to the general argument of the paper, reflects widely held opinion among workers in this area. In the section aded "Selection Methods," Gorn remarks:

> Distinguishing "routines" from "live" or "intelligent" behavior depends not so much on their simulation of decision making or thinking but on their completely deterministic pattern.
>
> Most routines do simulate "routine" thinking, as opposed to "executive" thinking in which creative or random choices of alternatives are involved.

suming that "intelligent" is not taken as synonymous with "adap- ve," the connection between random selection and "creative think- g" has never been convincingly established. We should rather sug- st that it is the depth and complexity of the decision process and t its indeterminateness that distinguishes from the routine that be- vior which people generally catagorize as intelligent.

The paper "Two Notes on Machine Learning" by Martens is a laud- le, if not conspicuously successful attempt to shave some of the fuzz m the hairy subject of learning automata. Note 1 describes the gital computer representation of a simple but interesting machine that is able to learn to play finite 3×3 board games (the examples discussed are tic-tac-toe and a pared-down version of Hex). Satisfied that this machine exhibits the essential features of a learning automaton, Martens, in Note 2, constructs a plausible formal description of a class of automata for which his learning machine is a possible interpretation. Unfortunately, the formidable formal structure produced begets only one quite trivial theorem. It would not be surprising, however, if extension of this work were to yield some more interesting results.

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Pattern Recognition and Reading by Machine—W. W. Bledsoe and I. Browning. (*Proc. EJCC*, Boston, Mass., pp. 225–233; December 1–3, 1959.)

This paper warrants close study by the serious student of character recognition; unfortunately it will require such study to discern its value. The schema is proposed for the recognition of typewritten, hand-printed, and separable hand-scripted characters by an ingenious variation of template-matching which does not succumb wholly to the temptation to standardize size, position, or orientation. The technique appears to be relatively general and applicable to other problems than alpha-numeric recognition. In common with other variants of template-matching, it will be troubled by registration and orientation to some extent. The most trivial form of template matching memorizes the occupancy matrix (for a quantized retina) of every pattern presented. The authors along with all other workers reject this approach in favor of examining a more limited sample of the occupancy matrix. Previous workers ("Solartron"[1] at Farrington, Wada,[2] and Dimond[3] among others) have sought and used these elements of the occupancy matrix which are occupied in common by all patterns of the same symbol. Much effort has been exerted by these earlier workers toward finding an optimum set of such occupied elements. The authors of this work make the simple addition of recording both the occupied and unoccupied elements of the retina for n-tples of randomly chosen visual elements and correlate a number of such n-tples to test each new chapter against the results of pat experience. Evidence is presented on learning as a function of the number of elements in the n-tple, when a 10×15 occupancy matrix is used. One of the most provocative tests left undone is to determine whether a careful selection of the n-tple elements would aid the recognition process. No use is made of the fact that some of the n-tples more or less frequently occur for each exemplar.

The authors make a number of preliminary tests which will be of interest to others, such as recognition by combinations of canonical shapes, the use of the confusion matrix as a discriminant (called "distribution processing" in the paper), and show the value of avoiding a final decision on each symbol until the context of symbols is examined. The paper is marred by the use of poorly defined terminology; *e.g.*, calling the translation of the pattern along x and y axes in symmetrical steps a "rotation," discussing the averaging of matrices without defining the term, using "alphabet" for both sequence of symbols and set of exemplars of such symbols.

The experimental data leave more questions unanswered than one would like. Typewritten text is dismissed in three sentences distributed through the paper as being recognizable 100 per cent of the time "under all conditions *tried*" (mixed pica and elite, mixed capital and small, degree of misregistration, ?). Fig. 10 quotes mean recognition of hand printed block characters as 78.4 per cent with a standard deviation of 1.0 per cent for randomly chosen 2-tples while Fig. 6 shows recognition percentages which never reach these heights for five differing collections of samples. Fig. 8(b) was totally obscure to the reviewer. It is implied, but never stated, that the percentage of false recognitions was 100 per cent minus the per cent of correct recognitions. Confusion matrices are not shown. Finally it would be well to point out that character recognition has achieved the status where one should state the number of different sources from which hand printed and script samples are being recognized and whether the source of both learning samples and test samples are the same or different.

[1] Reported in the discussion of Wada.[1]

[2] H. Wada *et al.*, "Electronic Reading Machine," *Proc. Internatl. Conf. on Information Processing*, Paris, France, June 15–20, 1959, Columbia University Press, New York, N. Y.; 1960.

[3] T. L. Dimond, "Device for reading handwritten characters," *Proc. EJCC*; Washington, D. C., December 9–13, 1957; pp. 232–238; 1957.

The techniques used are closely related in principle to those used by Roberts[4] and the Cornell Aeronautical Laboratory Group[5,6] whose "accumulators" are nonlinear versions of Bledsoe and Browning's "n-tples."

The lengthy quibbling with details should convey the reviewer's impression that the paper is worthy of such careful study. The correct recognition scores are strikingly good considering the simplicity of the method.

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[4] L. Roberts, "Pattern Recognition with an Adaptive Network," 1960 IRE International Convention Record, Pt. II, pp. 66–70.
[5] Hay, Martin, and Wightman, "The Mark I Perception" 1960 IRE International Convention Record, Pt. II, pp. 78–87.
[6] F. Rosenblatt, "Perceptron simulation experiments," Proc. IRE, Vol. 48, pp. 301–310; March, 1960.
[7] Reference added by editor in proof:
W. H. Highleyman and L. A. Kamentsky, "Comments on a character recognition method of Bledsoe and Browning," IRE Trans. on Electronic Computers, vol. EC-9, p. 263; June, 1960.

Perceptron Simulation Experiments—Frank Rosenblatt. (Proc. IRE, vol. 48, pp. 301–309; March, 1960.)

This paper, written by a researcher formally trained in one of the behavioral sciences, is concerned with the use of a digital computer to simulate perceptual learning and recognition of visual stimuli in a "perceptron." A perceptron is a theoretical model dealing with the noise-free logical functioning of those portions of the mammalian brain that are presently considered to be concerned with sense-perception. The computer-simulation of the "perceptron" is in the sense of some reasonable but contested characteristics of the logical functioning of the mammalian visual system. To this extent the "perceptron" cannot be considered the last word on a model for the brain. In addition the reviewer wonders to what extent the choice of characteristics referred to above was motivated by an *a priori* knowledge of the nature of digital computers? Did this choice affect the theoretical model itself?

An investigation of a "perceptron" falls within the domain of study dealing with what is called artificial intelligence. In this respect refer to the later works of A. M. Turing.[1] In turn, artificial intelligence falls within the scope of a study of general self-organizing systems.[2,3]

To date the most successful use of a simulator for a "perceptron" has been in the role of a pattern-recognizer, although rudimentary aspects of learning have been demonstrated, too. But, it appears to the reviewer that if the "perceptron" project was not primarily an investigatory one, then a practical pattern-recognizer could be had with considerably less effort and expense than with a "perceptron"-simulator. Then, again, if one was primarily interested in the more general aspects of a study of self-organizing systems would one really want to go around simulating things on a digital computer?

In conclusion, the reviewer believes that Rosenblatt has expounded an interesting and coherent account of nearly three years of research on the theory and simulation of "perceptrons."

Erratum: Hebb's book, as listed in the bibliography, should be dated 1949 rather than 1959.

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[1] S. Turing, "A. M. Turing," Heffer and Sons, Cambridge, England, 157 pp.; 1959.
[2] M. Yovits and S. Cameron, eds., "Self-organizing Systems," *Proc. of an Interdisciplinary Conf.*, Pergamon Press, New York, N. Y., 375 pp., 1960.
[3] S. N. Braines, A. V. Napalkov, and Yu. A. Schreider, "Analysis of the working principles of some self-adjusting systems in engineering and biology," *Proc. Internatl. Conf. on Information Processing*, Paris, France, June 15–20, 1959. Columbia University Press, New York, N. Y.; 1960.

Penny Matching Machines—Gerald M. White. (*Information and Control*, vol. 2, pp. 349–363; 1959.)

The author analyzes a penny matching "game" between a player and an "indifferent opponent" whose play is independent of the outcome of the game. Two classes of opponents are considered; class B (Bernoulli) has fixed probability of playing heads and class M (Markov) has probability of heads conditional on the previous play. In both cases the probabilities are initially chosen from a distributio and are not changed during a game.

The results are not surprising. Against B the player should alwa play so as to win if B were to make his higher probability choic If the player treats M as if he were B, in certain cases he is wor off than if he treats M as M.

"Thus, this paper containing a discussion of a player having simple criterion playing a simple game against a simple opponen serves only as an introduction to a very complex field."

Considering the results achieved for the effort expended and th gross simplifications used, it seems to this reviewer that more powe ful methods will be needed before the problem of "the design machines capable of making decisions" is solved.

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Alpha-Numeric Character Recognition Using Local Operations—J. S. Bomba. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959, p 218–224.)

This paper expounds a method for alpha-numeric charact recognition which falls into the class of special feature recognitio and programs. The author limited himself to the recognition and e traction of straight lines with varying tilts and V, T, and L inte sections with various amounts of rotation. The limited class of fe tures unfortunately requires a further designation of the position each of the features within the visual field. It would seem th marking the relative position of features with respect to one anothe rather than absolute location within the visual field, would hav removed the size and position intolerance of this technique. Th absolute location of features makes the process sensitive to size ar location within the 60×90 visual matrix. The author reports a to erance of about two to one for allowable size variations and lit thickness variation.

Preprocessing is used to filter out stray noise and to standardi line widths. The author mentions that serifs and other decoration will create problems for his techniques. Since the serifs and oth decorations usually have a certain uniformity, it would again see that the preprocessing might be used to filter such decorative add tions.

The decision process is taken through a logical tree to the symb which satisfies each of a number of sequential decisions. Of all th pattern recognition techniques, the special feature recognition pr gram lends itself most gracefully to a parallel rather than serial d cision process. The advantage of the parallel decision process lies the possibility of making errors in individual feature recognitio without catastrophic effects on the final symbol recognition.

This paper is another in a series of recent publications whic points up the need for a learning program which will examine number of exemplars of the same symbol for those special featur which will be most helpful in establishing the symbol and distinguis ing it from other symbols.

The paper is reticent on the statistical performance of the pr gram except to say that three sample alphabets were recognized.

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D. Digital Computer Systems

The Multi-Sequence Computer as a Communications Tool—J. N Ackley. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959, pp. 114 119.)

Computer techniques as applied to a Communications Switchin Center are briefly discussed. They range from the use of an externa control device (Data Synchronizer) with storage for buffering an control words to the use of the main computer memory for this pu pose. In the Data Synchronizer approach, only a single memor cycle is needed for a transfer, whereas in the latter case, a large po tion of the computer capacity is tied up in input/output transfers.

A system is then described which by multiplexing a Centra Computer can handle a large number of communication lines. "multi-sequence" configuration is utilized which provides a numbe of program counters and means for the switching from one counte to another, in response to an external command. In this fashion, th transfer from one multiplexing "sequence" to another is accom plished.

The priority scheme used assigns a priority to an input channel permit the handling of devices operating at different speeds and provide an orderly procedure for the handling of requests. Independently, a priority can be assigned to a particular message.

The reviewer would have preferred a more detailed description the System. For example, the method of error detection and correction which is of particular interest in the design of a Communications Switching Center was completely omitted in the paper.

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nputers of the Future—Rex Rice. (*Proc. EJCC*, Boston, Mass., ember 1–3, 1959, pp. 8–14.)

This paper indicates how computer technology might advance n its present stage, through successive generations of machines, point at which microminiaturized computer systems, comprising ronomical numbers of microscopic components, will be both deed and manufactured by automatic, computer-controlled proces.

Extension and improvement of present techniques for mechanizan of the design process, together with automatic fabrication cesses, will make it economically feasible to use many more nponents in complicated logical structures in the next generation machines after the present ones. In the generation after that, cial purpose systems will be built using the multi-element coments, such as counters and registers, which will be in common by that time. In the third generation following the present one, multi-element devices will handle major system functions, and k storage will be entirely internal. From this generation will lve the machines mentioned in the first paragraph, which will ude a measure of self-organizing ability.

Accompanying the above developments will be changes in several ects of computer design and use. Maintenance techniques will nge, as more and more redundancy is included in the logic, and ger and larger segments will be considered "replaceable packages." entually "maintenance" will consist of discarding the entire mane if it malfunctions. The ease and convenience of programming l increase as the machine language approaches successively closer human language. This will not, however, reduce the problem of ing the machines the proper questions. Design techniques will nge also, with greater emphasis being placed on standardization l systematic layout, and less on the number of components or logical complexity.

This paper emphasizes the close relation among changes in comnent speed, component size, the interconnection problem, mechzation of design, and automatic fabrication processes. It raises for individual the question "How do I extend my present specialized lls to encompass all the fields of system synthesis, logic design, cuit development, and device design?"

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gineering Design of the STRETCH Computer—E. Bloch (*Proc. CC*, Boston, Mass., December 1–3, 1959, pp. 48–58.)

It is a very difficult task to present one of today's giant computer tems in a short paper. Bloch, in his talk about STRETCH, has ne a very good job describing both system and components in a mprehensive and careful way.

STRETCH, custom designed for Los Alamos, is without doubt fastest and most complicated system now available. Among its ent features are:

1) A very large (max. of 256,000 words) 2-μsec 64-bit core memory, of modular organization, which allows a very high memory reference rate.
2) A look-ahead unit, operating on 2 instructions and 4 data in advance, doing most of the bookkeeping and updating concurrently with computation, and allowing, therefore, the overall computation rate to be substantially increased. The logic of the look-ahead unit is quite complex, and includes 15.6 per cent of the total transistor count.
3) The possibility of operating on variable-length fields; the field may cross the word boundaries and has a maximum length of 64 bits.
4) A very fast arithmetic unit (floating addition 1 μsec, floating multiplication 1.8 μsec on 48-bit fractions). The compression of multiplication time is made possible by a recoding of the multiplier in groups of 3 bits, and by addition or subtraction of even multiples of the multiplicand at every step. The division scheme is based on Robertson's division algorithms.
5) An interrupt system, which however, is not described in the paper in full detail.
6) An Exchange element, linking the memories to input/output, which runs independently of the central computer. Among the I/O units is a very large disk memory of 4×10^6 words with a 4-μsec exchange rate.

The basic logical circuit uses high gain-bandwidth transistors in "current switching" configuration, which allows higher speeds by keeping transistors out of saturation. Propagation time is between 12 and 25 nanosec per logical step. The logical chains are formed by alternating stages of PNP transistors with NPN transistors.

The 169,000 transistors in STRETCH are mounted on 22,000 cards, contained in 18 frames. Special care has been used in packaging and wiring design to minimize electrical noise. The frame background wiring is laid on a ground-plane; power supply voltages are distributed by laminated copper busses; long signal wires are twisted pair or coaxial cable.

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Design of Univac-LARC System: I—J. P. Eckert, J. C. Chu, A. B. Tonik, and W. F. Schmitt. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959, pp. 59–65.)

In the opinion of this reviewer, the objectives of describing the LARC system adequately are not met by this paper. No detailed block diagram or operation times are given; the description of the system is always very general; therefore, when the authors state that they "pressed the limit of the art at the time the design was frozen," the reader does not have any valid check on their statement. The authors declare further that LARC is well-balanced, because it obtains the greatest work output for the cost involved: since neither the cost, nor work outputs are quoted, again the reader is asked to have faith. On the other hand, this paper is much more a progress report on the project than an exposition of the design philosophy, which may be found in a number of papers written since the LARC design was started.

LARC can claim many firsts in system design; some features in its logic were quite revolutionary four years ago. It is a pity that hardware development has delayed the completion of the computer. It is interesting to note that the old argument of "binary vs decimal" is still not solved, since LARC is a decimal machine, designed to carry on scientific computation.

Basically, the LARC system consists of a computer and a Processor: both units are controlled by stored program. The Processor handles input-output devices, does control input-output data conversion, editing, sorting and merging. The operation of the Processor is initiated by control words from the computer; the Processor is then free to run its own program independently. Processor and computer share a common pool of magnetic core storage modules. A second computer can be added to the system, so that two computing units can operate on one or two different problems simultaneously. The degree of interference between the two computers is not explained in detail.

Very little is said about the computer itself, so that one does not have any element to judge its design. There seems to be a large number of fast registers (100), operating on a 1 μsec cycle; some of them specialized. It would have been very interesting to know how they are interconnected, and what degree of flexibility they allow to the programmer.

The core store has been made modular in construction, to increase the reference rate. The present 20,000 word capacity can be expanded to 100,000 12-digit words; the modules each contain 2500 words, and have a 4 μsec cycle time.

The memory requirements are completed by drum units (transfer rate of 500,000 decimal digits/sec), and tape units (25,000 alphanumeric characters/sec).

Among I/O devices, it is worth noting:

1) An on-line electronic page recorder, using a CRT and microfilm at 20,000 characters/sec.
2) Electro-mechanical on-line printers at 600–700 lines/minute; the printer synchronizer can be used with fast printers, up to 1200 lines a minute.

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Design of Univac-LARC System: II—H. Lukoff, L. M. Spandorfer and F. F. Lee. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959; pp. 66–74.)

This paper presents many of the engineering considerations in the design of LARC. The basic logical circuit was selected with a very simple formula:

$$(\text{figure of merit}) = \frac{(\text{drives})\ (\text{logic levels})\ (\text{repetition rate})}{(\text{transit time})\ (\text{cost})}.$$

The simple transistor-diode circuit performs NOR logic; transistors are Philco surface-barrier. The worst core transit time through one logic level is 40 nanoseconds; pulses are reshaped and retimed every 9 logic levels. A synchronous system was selected because the faster asynchronous operation advantage was offset by an increase in hardware and complexity. The authors have a very strong point in favor of synchronous operation, namely debugging and maintenance case; many of the readers will agree with them.

Circuit components are mounted on high density cards. Since every card connector has 42 pins, and connectors occupy 88 per cent of the backboard wiring area, the wiring density is very high. Therefore, taper pins wire connections were adopted. Special tools had to be developed to facilitate the wiring task. A "boroscope," for example, gives the wiring technician the possibility of looking closely at the connectors through the jungle of wires.

Wiring charts have been produced by computer program. Automatic techniques to accomplish this task are almost indispensable in large systems; the problems involved are not as trivial as they may seem, especially if one wants an "intelligent" program to check part of the design, eliminating the inconsistencies, and to minimize noise, by reducing wire lengths.

Checking of the circuits is accomplished by varying the collector-return voltage to determine the beta-margins. The voltage is varied over a whole unit, and a weak circuit may then be located logically by error-detecting circuits scattered throughout the machine.

62,000 transistors and approximately 170,000 diodes are used in LARC.

Readers interested in fabrication techniques will find this paper very interesting. Many useful tricks of the art are explained in detail: especially in large systems, where one cannot afford to fabricate in a clumsy way, those are at least as important as a sound system design, and a great deal can be learned from other people's experience.

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1) A Universal Computer Capable of Executing an Arbitrary Number of Sub-Programs Simultaneously—John Holland. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959; pp. 108–113.)

2) Iterative Circuit Computers—John Holland. (*Proc. WJCC*, San Francisco, Calif., May 3–5, 1960; pp. 259–265.)

These papers present an interesting new computer species introduced by Holland primarily to provide a vehicle for his theoretical study of adaptive systems. Paper 1 gives a general description of a particular specimen, while paper 2, after giving an abbreviated but slightly broader version of this specimen, proceeds to a mathematical characterization of the species and indicates how it can be used to investigate adaptive behavior deductively.

Apart from the usefulness of these computers as theoretical models, they include organizational concepts that are significant and challenging both for the machine designer, interested in expanding the processing power of his machine, and the device engineer, searching for a fruitful course in hardware development.

The basic structure and the rules of operation that Holland has selected for his machines enable simultaneous activity of a varyin number of programs in the system; programs may be directly co trolled from the input as well as from other programs with whic they interact. The specific machine described in 1 and 2 is a homo geneous 2-dimensional rectangular array of computing modules, eac of which contains a binary storage register, together with circuitr for interpreting and executing instructions as well as for controllin communication with adjacent modules. A word in the storage regist is interpreted either as an instruction or as a datum, depending o the status of the module, which in turn is determined by auxiliar registers contained in the module. Storage registers and auxiliar registers are directly accessible from the input, once in each operatio cycle, thus enabling a strong dependence of the course of processin to signals from the environment. A module in active status, E-modul interprets the contents in its register as an instruction and contro its execution. Part of the instruction specifies to which of the fou adjacent modules program control activity should be transferred unless the instruction directs a "jump" to a specified, and generall nonadjacent set of modules. In this latter case more-than-or branches of program control activity are created from a sing branch. The graph of consecutive E-modules corresponds to a pr gram. Each module in the graph assumes the combined conventiona functions of a program register, an HSM instruction word, an addre register, an operation register and a control decoder. The operan relevant to an instruction as well as the arithmetic unit to be use with them are located in modules that can be reached through we defined paths from the E-module that carries the instruction. Pa of the instruction specifies the length and the directions of the pat segments that lead to the operands. The construction of path star from a module that has a special status, and is located on the branc of the program graph that precedes the E-module. Another modu in a different special status, also located on the same branch of th program graph, assumes the function of an arithmetic unit. Th essential difference between the machines described in papers 1 an 2 is that in 1 a single operand per instruction is considered while considers a multi-operand machine, with provisions to combine th set of operands into a single one before feeding it to the arithmet module. In paper 1 eight basic orders are considered, covering add tion, data transfers, control of program sequencing and path building paper 2 gives a representative subset of these orders suitable fo multi-operand processing. Paper 1 describes a set of interlockin conditions that regulate the activity of program control, path build ing and processing as it evolves simultaneously in different progra graphs, distributed spatially over the system.

The general mathematical description of the computer specie given in paper 2, implies that, besides the requirement of structura homogeneity at large, one can choose a machine of any number modules, where each module has an unrestricted number of neigh bors, it can have registers of any size, execute various desired opera tions and form paths of different types. However, if construction such machine is considered using present advanced planar manu facturing techniques, it seems that we can expect at best a bas structure in the form of a connected stack of honeycomb plane giving a neighborhood set of 8 or maximum 12 as a basis for progra branching and operand selection. The most serious restriction such machine with respect to present designs lies in the scheme fo selecting operands. Selection is not made from the totality of storag registers and is based neither on absolute coordinates nor on "name" for the contents, but on a relative position with respect to point in the program segment previously executed; the set of op erands that can be reached at any cycle in a program is only 8 time the maximum length of a path segment, for a simple honeycomb stacked system. This mode of selection gives a vast importance t the relative positioning of information over the structure and thu creates a formidable problem of data allocation. Other problem result from the rigidity created by specifying a unit-module with fixed storage and switching capacity. For instance, processing messages exceeding in length the capacity of a storage register need special programming. A provision for making teams of modules t operate as a single one would solve the problem of variable messag length, and in general would increase the functional homogeneity i the machine. Newell has suggested first solutions both for the prob lem of teaming modules and for the problem of "associative" selec tion of operands in a Holland machine;[1] however much more need to be done in these areas. It should be pointed out that for any finit

[1] A. Newell, "On Programming a Highly Parallel Machine to be an Intellige Technician," *Proc. WJCC*, San Francisco, Calif., pp. 267–282; 1960.

achine the "arbitrary" number of programs that can be processed multaneously must be bound by a theoretical upper limit. This mit depends on the nature of the programs and their distribution ver the machine and it probably can never be reached in actual peration.

The limitation on data selection at each program step is one of the ecessary properties resulting from a fundamental concept in the roposed organization: lack of specialized organs and of central administration. The existence of the latter features is typical of efficient designs, evolved on basis of a high state of knowledge on the xpected tasks, and also on basis of appreciable concern over component economy. The cell-modules of Holland's machine are undifferentiated general purpose computers that may be called at different times to perform various partial tasks involving only a raction of their processing potential. In addition, it seems that the oal of program design for complex parallel information processes on uch a machine will be primarily to attain *feasible solutions* rather han to find optimal ones, in the sense of minimizing for instance the umber of idle cells in the system. Therefore construction of Holand's machine strongly depends on availability of equipment with ost functions that are weakly dependent on the amount of logic in ach module and on the process of stacking modules. Recent progress n the area of functional microminiaturization, specifically in techiques for manufacturing integrated electronic devices,[2] give hope hat such equipment will be available in the not too distant future. he relevance of microminiaturization techniques to the system under discussion is recognized by the author, as well as by the organizers f the WJCC, that have included paper 2 in a session on Design, rogramming and Sociological Implications of Microelectronics. lowever, it should be recognized that although microminiaturization echniques will be essential for the construction of Holland's mahines, the concept of these machines is not necessary and most robably was not evolved in order to satisfy organizational requirements of microminiature hardware; it evolved rather in response to n operational request for highly parallel processing and for self rganizing, adaptive behavior.

Current interest in parallel processing of parts of well formulated roblems in a single system comes from a desire to increase the tilization factor of a single computer or from the need to efficiently xecute tasks beyond the processing power of a single computer. he problem of scheduling parts of programs to separate processors s a difficult one and still necessitates considerable research on proram structures and on automatic techniques for program decomosition. Addition of spatial constraints to the existing constraints f logical order make the task of multiprogramming a Holland mahine look truly difficult. It is unfortunate that the author did not resent a simple example of interacting programs to illustrate the roblems involved. The difficulty of programming and the inefficient tilization of hardware make Holland's machine less attractive for rocessing well formulated problems than an assembly of relatively onventional processors with a central administration of the type of BS' Pilot for instance. Of course, if the neighborhood relations etween modules are homomorphic with ordering relations between ariables in the problem space, processing with an iterative machine eems advantageous. This was illustrated by Unger[3] with his spatial omputer, whose rectangular iterative structure suggests similarity ith Holland's computer. However, in Unger's computer a single nstruction is simultaneously executed by all the modules in an rray, on which a visual pattern is mapped; program control is exernal to the array. A Holland machine would hardly be suitable for uch a uniform task as its forte would be in analyzing a visual pattern y simultaneously carrying out different tests and local transformaions at different points, or, in general, in representing a space ruled y a great variety of forces at different points.

Holland's iterative machines seem particularly suitable for comlex processes with ill-defined solutions, where the construction of rograms is a gradual process carried out by the machine itself, hrough interaction with environment and learning. Emphasis in his area is on extreme flexibility of structure rather than on comonent economy, on initial homogeneity and local autonomy rather han biased and specialized organs and on the discovery of an cceptable solution rather than the optimal one. The suitability of he iterative computers for adaptive self-programming was not made as explicit in paper 1 as in paper 2, where this is clearly implied from the description of the investigation in adaptive systems in which the postulation of the iterative computers is an initial step.

This investigation seems to be an extension of the study on growing automata[4] carried on at the University of Michigan; an important aim of the study is to consider different specific types of automata having variable structure, to find languages in which these automata can be represented and to investigate their significant properties. An example of such an approach to the study of adaptive structures, adopted recently by many researchers, is to postulate an artificial neural net with changing thresholds and synaptic values and a specified connectivity, based on some biological plausibility, and to find analytically as well as by simulation significant behavioral properties of the net operating in adaptive modes. Holland's approach is similar, only he postulates a different variable structure, the iterative computer, built of conventional digital computer circuitry, and he also provides a language for its representation. He indicates in paper 2 that his next step is to choose "automata generators" in the form of molecular programs and rules of interaction between them so that any particular automaton-program can be obtained by controlling the interaction of molecular programs. He intends then to define the term "adaptive system" implicitly in terms of generators embedded in an iterative computer and their interactions, so that a deductive investigation of the defined system will be possible. In other words, a complex variable structure will be formally constructed and named an "adaptive system" with the purpose of looking later into it and discovering its behavioral characteristics. There is no biological backing to Holland's postulation, and a serious evaluation of its usefulness can be made only at a later stage when it can be seen how fruitful it has been for generating kinds of behavior that we can call adaptive. A major objective of the line of investigation taken by Holland is to have all along a mathematical metalanguage for expressing the system's operation so that an experimental investigation of the system is not necessary. In fact it is pointed out in paper 2 that it will be desirable, for the sake of the formal treatment, to have also implicit definition of the environment. This is certainly good research strategy, but it is a sensitive point and should be handled carefully since one of the important functions of a learning system is to discover an implicit representation for its environment. The real test for the mathematical representation of the iterative structure, presented in paper 2, will come at a later stage, when it will be used to express relationships between structures and behavior and to clarify specific questions about system operation. Most of the difficult work is yet to come and it is hoped that the ground cultivated so far will bear fruit in the future.

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[2] J. T. Wallmark, "Design considerations for integrated electronic devices," roc. IRE, vol. 48, pp. 293–300; March, 1960.

[3] S. H. Unger, "A computer oriented toward spatial problems," Proc. IRE, ol. 46, pp. 1749–1750; October, 1958.

[4] A. W. Burks, "The logic of fixed and growing automata," *Proc. Internatl. Symp. on the Theory of Switching*, April, 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 29, pp. 147–188; 1959.

Review to appear in December, 1960 issue.

Arithmetic and Control Techniques in a Multiprogram Computer—N. Lourie, H. Schrimpf, R. Reach, and W. Kahn. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959; pp. 75–82.

This paper is concerned with two unrelated topics in computer engineering: a time-sharing control system and a form of semiparallel adder. The only relation between these two subjects is that they both form bases of design methods incorporated into the Honeywell 800 System. According to the authors, the objectives of these design techniques were to help achieve "better machine performance for little or no increase in cost." The design methods themselves are briefly described in the paper; whether or not they meet the stated objective is not fully evaluated by the authors, although various plausibility arguments are given toward this end. In this reviewer's opinion, however, the methods certainly seem worthy of consideration.

Few papers that discuss control methods in any detail have appeared in the literature, but multiple-unit computers and multiple-program computers have been described.[1] The control concept discussed in this paper is that of the latter type, where the computer

[1] See, for example, R. S. Ledley, "Digital Computer and Control Engineering," McGraw-Hill Book Co., Inc., New York, N. Y., ch. 8; 1960.

executes several (up to eight) different programs at once by interleaving the successive instructions of each program. That is, the computer will execute an instruction from the first program, then an instruction from the second program, etc., until an instruction from each program has been executed; then the next instruction from the first program would be executed, and so on. Several exceptions to this procedure required for various operations are discussed. The process is carried out through the use of an auxiliary memory, which holds a current address counter for each of the programs. This same memory is used to control up to eight peripheral input-output devices. Other analogous uses of the memory are also described.

There are many advantages to the "time sharing" of several programs at once; these, however, the authors did not elaborate. For example, by this means several programs could be debugged simultaneously. Of course, a supervisory routine could be formulated to enable an ordinary computer to time-share programs—hence the question arises: It it worth designing such a time-sharing feature into the computer? Consider again the debugging example: Here, certainly, built-in time sharing will be of great advantage. Yet even with built-in time sharing, a need still arises for a supervisory routine to insure that the debugging procedures for one of the programs will not change the contents of addresses used by other programs. Thus the efficacy of the built-in feature depends to a large extent on the amount of extra circuitry required. For the case described in the paper, it appears well worth while.

The second topic considered in the paper is the logical design of an adder, utilizing a "parallel-serial-parallel" format, for providing "fast arithmetic speed at a relatively economical cost of logical circuitry." The operation of this adder is described. The adder consists of three four-bit parallel adders, each of which adds 16 bits in four serial groups of four parallel bits. The three parallel-serial adders operate in parallel with each other, and in total a 3×16 equals 48-bit adder results. This design appears effective in the case described, although insufficient analysis of its utility or advantages was presented in the paper.

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E. Circuits

Solid State Microwave High Speed Computers—Jan A. Rajchman. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959; pp. 38–47.)

Phase locked oscillators and tunnel diodes are receiving a good deal of attention with regard to their application in ultra high speed computing machines. This presentation was a qualitative survey of RCA's efforts along these lines.

A brief discussion of the mechanism by which subharmonic oscillators are built up and sustained was presented. More detailed analyses have been presented and published elsewhere. The schemes of Goto and vonNeumann were applied to implement logic at microwave frequencies with phase locked oscillators. The author stated that in order to achieve 1 kmc information rates, with practical logic gains, a pumping frequency of 30 kmc or higher would be required. Several oscillator configurations in strip line were presented. Using microencapsulated diodes, constructed specifically for use with strip line, phase locked oscillators were operated at a 10 kmc pumping frequency with a rise time of 2 to 3 nsec and efficiencies of 10 per cent. The use of linear summing networks, such as the hybrid ring, to perform logic was also briefly discussed. A binary adder was given as an example of the application of these transmission line networks.

The author also discussed tunnel diode characteristics and their application in logic circuits. Three types of logic elements were described, all of which used a clocking scheme for achieving unidirectional logic flow rise and fall times of 1 nsec were reported. The author holds great promise for this device to achieve kilomegacycle logic rates.

Tunnel diode memories were also considered in this paper. The memory arrays discussed consisted of constant current driven bistable tunnel diode circuits located at each intersection of an X-Y matrix. The circuit is coupled to each line by resistance and selection is obtained by coincidently passing current into the selected diode to interrogate it. The destructive read-out schemes consisted of direct pickup of the switching transient on a common line or transient excitation of a tuned circuit loosely coupled to a common line. An interesting nondestructive read-out technique was described whereby one uses the difference in the nonlinearity of the diode characteristic at the two operating points to effect the magnitude of a beat frequency. The diode is interrogated by two sinusoidal voltages of different frequency. The variation in the amplitude of the difference frequency obtained in stable state 1 to that obtained in stable state 0 is used to determine the state of the diode being interrogated. Operation at a difference frequency of 1 kmc was reported.

The author concluded his presentation with some remarks about packaging, power dissipation and signal transmission delay in a machine to operate with nanosecond logical delays and a 10-nanosecond memory cycle.

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High-Speed Switching by Rotational Remagnetization—Herbert B. Callen. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., pp. 179–185; 1959.)

The achievement of millimicrosecond switching speeds using magnetic films and switching fields of a few oersteds was the culmination of an extended (roughly 1952–1956) experimental and theoretical effort in which a number of workers at different laboratories made important and successive contributions. Millimicrosecond magnetic-film switching is now common knowledge, and for people who are not specialists in this field, no better simple explanation of the general physical reasoning underlying this phenomena is known to this writer. An estimate of switching speed is first made which omits damping, followed by a short discussion of the damping problem. This latter problem is a difficult one which is attracting much attention from physicists and the simple account given here is certainly not the final story. Nevertheless, as an indication of one method of approach this discussion should be interesting to the nonspecialist. Because of the generality of the treatment some of the essential elements of the specific problem at hand are understandably not dealt with, in particular the role of the "transverse" field.

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Deposited Magnetic Films as Logic Elements—A. Franck, G. F. Marette, and B. I. Parsegyan. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959; pp. 28–37.)

Thin magnetic films have been developed in the past few years for digital memory applications. This paper discusses some methods of using thin magnetic films to perform logic.

The authors describe two modes of operation which result in logical gating. In the "reversible rotation mode" two perpendicular fields influence the film and an output occurs only when both fields are present. In the "saturable transformer mode" the input fields are parallel and an output occurs whenever the net field exceeds a threshold field. Rectangular arrays of the thin film logic elements which will perform logical operations are described. Most of the text is devoted to these "functional array" devices. Parallel logic methods are used to decrease the computation time.

The thin film logic device makes use of two special properties of thin films. First, the influence of a field perpendicular to the direction of magnetization is used to rotate the domain orientation. Second, this rotation can be sensed in an output loop whose plane is parallel to the field which is causing the rotation. As a result the mutual coupling between the sense circuit and the drive circuit would be very small in the absence of the film. The "saturable transformer mode" makes use of only the first property while the "reversible rotation mode" uses both properties.

The logical operations which can be performed by a single thin film element are exactly those which can be performed by a single magnetic core or any other threshold device. We conclude that the *logical capabilities* of the film element are not unusual. Any logical operation which can be performed by n thin film elements can be performed by n magnetic cores in a similar fashion. However, the *physical capabilities* of the thin films are in some ways superior to magnetic core capabilities. In particular, the thin film rotation can take place in a very short time with reasonable applied fields. It is unfortunate that the authors did not present any information on the

rsical characteristics of the film elements. The mode of operation cribed is based on an idealized characterization of the film be- ior. Well-known experimental results show that the idealized lel is inadequate when the film is subjected to large transverse ls as it is in the "saturable transformer mode." The "functional ays" may be accurately described as conventional parallel logic uits arranged on a rectangular grid. The speed advantage which allel logic has over sequential logic is common knowledge.

An evaluation of the thin film as a logic element is not possible in absence of information on the physical characteristics of the film ments. However, some points which will be significant in the luation can be cited.

1) The thin film rotational process is very fast and involves low internal losses so that high repetition rates are possible without severe heating.
2) The array logic methods will impose stringent signal-to-noise ratio requirements on the individual elements.
3) A very large power attenuation takes place between the input circuit and the output circuit. As a result it will be difficult to maintain a good signal-to-noise ratio and multistage sense amplifiers will be required. The attenuation for the film elements described in this paper is about 60 db.
4) Although the thin film itself requires only a very small amount of energy, the power level in the drive circuit will be difficult for high speed transistors to achieve.

The authors have provided us with an early report in a field which rtain to receive great attention because of the high speed capabil- s of the thin film rotational process.

It would have been more consistent with the spirit of such an nouncement for the authors to report the physical characteristics the suggested logical element.

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rticle Information in Magnetic Recording Tapes—J. G. Wood- rd and E. Dellatorre. (*J. Appl. Phys.*, vol. 31, pp. 56–62; January, 60.)

The authors have attempted to throw some light upon the funda- ntal processes involved in magnetic recording by considering the ording medium to be made up of an aggregate of single domain gnetic particles with square loop characteristics in which the ect of particle interaction would be to make the particular loop mmetrical. They are particularly concerned with methods of alysis and experimentation which will indicate the nature and ent of this particle interaction. The effect of reversible magnetiza- n processes is disregarded as not contributing to the remanence.

The properties of the square loop particles are represented on an $-H_-$ plane where H_+ and H_- are the switching fields of the parti- s. In the absence of particle interaction H_+ and H_- for each rticle are equal in magnitude and they will fall along a 45° line in H_+–H_- plane. If particle interaction is significant, the square p for the particle will be unsymmetrical and $|H_+| \neq |H_-|$. In this e, the point locating the particle will lie off the diagonal. The mag- ude of the magnetic moment associated with a particle is repre- ted along a third m-axis perpendicular to the H_+ and H_- axes. e properties of an aggregate of such particles are represented as hree dimensional plot in (H_+, H_-, m) space. By a transformation, distribution can be related to the H_{ac} and H_{dc} fields of the an- steretic process common to magnetic recording.

Experiments were made using conventional recording equipment n which the distribution functions for two recording tape samples re deduced. The distributions were multihumped indicating the sence of significant particle interaction.

This approach represents a new attack on the fundamental proc- es in magnetic recording. The experimental results, while ex- mely interesting, are rather meager and any generalizations should approached with caution.

Although some time may pass before the distribution function ap- ach yields specific results in terms of improved recording mate- ls and techniques, it will be useful now in getting a better feel for fundamental processes involved.

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Microwave Logic—W. D. Lewis. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Harvard Computation Laboratory," Harvard University, Cambridge, Mass., vol. 30, pp. 334–342; 1959.

Traveling-wave-tube amplifiers and associated passive microwave components are capable of handling signals occupying bandwidths of at least 1000 mc. Dr. Lewis describes in this paper how this capability may be utilized to achieve digital data processing rates of up to 160 mc. By carrying the digital information as either AM or FM modulation of a microwave carrier, logic functions can be performed by suitably combining carrier signals. Loss of amplitude suffered in the logic networks can be corrected by the use of TWT amplifiers. When this paper was presented in 1957, the possibility of achieving a 160-mc pulse rate represented a major breakthrough in computer speeds. Since that time, there has been a flurry of activity to evaluate and to expand microwave logic techniques. The results of this activity have recently been published in these TRANSACTIONS[1] and elsewhere.[2]

Representation of a binary digit by the frequency of the carrier seems to be a rather complex way to handle a signal for logic purposes. The earlier proposal of Edson[3] to use multimode oscillators for memory may perhaps have somewhat more merit, especially if decimal numbers could be stored reliably in a 10-state oscillator. Inasmuch as the FM logic system proposed required balanced converters for the logic functions and various sizes of waveguide to carry the different frequencies, it would seem to be a less attractive system than the use of amplitude modulation. If the digital information is carried as 100 per cent amplitude modulation of the carrier, then relatively simple circuits provide the necessary logic function. The OR function, for example, can be achieved by a simple junction of lines. If a signal is present on either of two lines, there will be an output, but if two inputs occur simultaneously, they might cancel and give no output. This cancellation could be used to give the EXCLUSIVE-OR function, but would require very exacting tolerances on the phase and amplitude of the signals. Instead, the simple OR function was insured by predetermining the two signal amplitudes to be grossly different, thus avoiding the possibility of complete cancellation. This requires amplification to restandardize the signal after each such logic function. The other logic functions are achieved by combining baseband and carrier signals in modulators employing semiconductor diodes. Similar diodes detect the resultant modulated signal. The amount of experimental verification of these techniques prior to the publication of this paper is not clear, for no experimental data is given. It is known that at least the amplitude modulation system has been tested subsequently by various laboratories.

The author makes no strong claims for the virtues of a logic microwave carrier system other than the fact that very wide bandwidth amplifiers are available at microwave frequencies.

As predicted by the author, the capability of baseband circuits and devices has increased immeasurably in the intervening 3 years since his paper was presented. New semiconductor devices have been developed which can provide gain in baseband circuits with rise times of less than $\frac{1}{2}$ nsec (10^{-9} seconds). Though this speed does not rival the 30-db gain and 1–2-kmc bandwidth possible with a TWT, there is less delay in the semiconductor amplifiers. As stated in the paper, TWT amplifiers normally have 7–10-nsec delay. Although a technique is described to circumvent the repetition rate limit of 100–150 mc set by this delay, increasingly complex circuitry is required for an increase in speed of only two or three times.

We might ask then, what is the advantage of a microwave logic system. If the microwave carrier frequency is X band (10 kmc) or below, the components employed are large, bulky, and expensive. If the carrier frequency is considerably above X band, the components become smaller, but more expensive, and the signals are much more difficult to process. Certainly for a general-purpose digital computer, semiconductor logic devices seem much more appropriate. For certain applications, however, probably in communication systems where time delay and physical size are not critical, the techniques proposed by the author seem quite appropriate. This is especially true if the signals are already in the form of a modulated carrier.

[1] Several papers in IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, vol. EC-8; September, 1959.
[2] F. Sterzer, "Microwave parametric subharmonic oscillators for digital computing," PROC. IRE, vol. 47, pp. 1317–1324; August, 1959.
[3] W. A. Edson, "Frequency Memory in Multi-Mode Oscillators," Stanford University, Stanford, Calif., Tech. Rept. No. 16; July 19, 1954.

This paper presented new and novel concepts in the use of microwave carriers for achieving extremely fast digital circuitry. Because of pioneering efforts such as this, work on super-high-speed digital circuits has been greatly intensified. In the intervening years since the paper was presented, many different high-speed techniques have evolved. Each of the techniques developed will find application in the fields of digital data handling where its characteristics are best suited to the job to be performed.

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F. Memories

The Woven Cryotron Memory—Albert E. Slade. (*Proc. Internatl. Symp. on the Theory of Switching*, April 2–5, 1957, in "The Annals of the Computation Laboratory," Harvard University, Cambridge, Mass., vol. 00, pp. 326–333; 1959.)

The memory system proposed in this paper can be classified as a catalog memory[1] with permanently stored data. The data content of each of many words would be determined at the time of construction by the weaving pattern of word lines. These word lines would constitute cryotron gate circuits, each passing through one of a pair of control coils for each of n bit positions. One of the pair of coils represents 0 for that bit position and the other represents 1. Word lines (gates) would be tantalum wire and control coils would be wound with niobium wire. Operation would be at helium temperature.

The author proposes a construction technique which would permit the array of word wires to be arranged under automatic control of data from a punched tape. After making this arrangement, $2n$ control coils are wound around the gate wires at the appropriate points. Each pair of control coils would have all of the word wires passing through one or the other of the coils of the pair in accordance with whether a 1 or a 0 was to be represented for that bit.

For the simplest type of operation, the memory would be interrogated by placing current on the proper coils for the binary representation of the interrogating word. Any nonmatching word line would have at least one of its segments in the resistive state, while a matching word line would be super-conductive. With all of the word lines in parallel, the presence of a match or mis-match is indicated by the lack or presence of a potential drop across the word line circuit.

A more elaborate system would allow for the serial read-out of data associated with a matched identifying word.

With the limitations of a permanent memory and of the "yes" or "no" read-out for a match, the use would have to be very specialized to make the system worthwhile. It is unfortunate that the publication of this paper has been delayed for almost three years. In the meantime, interest in wire-wound cryotrons as computer elements has been largely replaced by work with thin films. At this point it appears very unlikely that the proposed woven memory would ever be built. However, the paper will be of interest 1) for its consideration of a "read-only" function table; 2) as one of the relatively few published papers giving cryotron circuits; and 3) for the catalog memory aspects of retrieving information associatively; that is, on the basis of its information content.

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[1] A. E. Slade and H. O. McMahon, "A Cryotron Catalog Memory System," *Proc. EJCC*, pp. 115–120; December, 1956.

G. Programming

Applications of Boolean Matrices to the Analysis of Flow Diagrams—R. T. Prosser. (*Proc. EJCC*, Boston, Mass., December 1–3, 1959; pp. 133–138.)

"Any serious attempt at automatic programming of large-scale digital computing machines must provide for some sort of analysis of program structure. Questions concerning order of operations, location and disposition of transfers, identification of subroutines, internal consistency, redundancy and equivalence all involve a knowledge of the structure of the program under study, and must be handled effectively by any automatic programming system."

The analysis of program structure with which the author is co cerned is that which can be readily performed on a large-scale digi computer. The author limits himself in this paper to questions connectivity in the flow diagram of a program; and properties of t individual boxes, representing program operations, are not co sidered. Using a computer program constructed for the IBM 7(appropriate matrices associated with a flow diagram are manipulat to obtain data of the following sort, for example:

1) boxes not connected to input (*i.e.*, can not be reached from t input in a finite number of steps),
2) boxes not connected to output,
3) boxes following a specified box,
4) boxes preceding a specified box,
5) boxes in a loop with a specified box, and
6) boxes which must precede themselves (*i.e.*, are inconsisten placed in the program).

This computer program can perform the above analysis on flow d grams which have as many as 500 boxes.

The author states that studies are currently in progress at Linc Laboratory " . . . to construct a completely automatic program a lyzer which would detect in suitably written programs a large cl of common errors, and then identify key subroutines and reorgan them into optional equivalent programs."

An automatic analysis of computer programs is almost a necess as the author indicates, and a modest beginning to the developme of adequate procedures is given in this paper.

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H. Reliability

A Note on Error Detection in Noisy Logical Computers—Murr Eden. (*Information and Control*, vol. 2, pp. 310–313; Septemb 1959.)

Using the works of von Neumann,[1] Moore and Shannon,[2] Elia and Peterson[4] as a point of departure, Eden considers a method error detection in finite automata constructed with error-prone co ponents.

In part, Eden's investigation is motivated by a comment of El to the effect that some of the results of von Neumann and Moo and Shannon produce certain anomalies when viewed in the light the principal result of statistical communication theory.[5] But i formation theory is not a panacea—and, after all, isn't the Moore a Shannon theory more of a unifying theory than an abstracti theory?—it deals with a calculus of probabilities, thereby treati conventional Boolean algebra and a theory of errors, together. Ho ever, the reviewer is enthusiastically looking forward to seeing so positive contributions made by information theory to stochas automata theory. To this extent the reviewer is of the opinion th historians will be hard put to determine whether the progress broug by the use of the concept of statistical independence in the first fif years of this century will match its braking-effect during the ne fifty years.

Considerable logical complexity will probably be introduced in a system-model which uses the component proposed by Eden. Ho ever, the reviewer would not feel bad to be proved wrong on th opinion.

Eden's paper gives some slightly more positive results th Elias' excellent paper, but the reviewer's over-all opinion of Ede interesting paper is that of St. John in his reference to The Lao ceans.

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[1] J. von Neumann, "Probabilistic Logics and the Synthesis of Reliable Orga isms from Unreliable Components," Automata Studies, Princeton University Pre Princeton, N. J., pp. 43–98; 1956.
[2] E. F. Moore and C. E. Shannon, "Reliable circuits using less reliable relay *J. Franklin Inst.*, vol. 262, pp. 191–208 and 281–297; September, October, 1956.
[3] P. Elias, "Computation in the presence of noise," *IBM J. of Res. and D* vol. 2, pp. 346–353; 1958.
[4] W. W. Peterson, "On checking an adder," *IBM J. of Res. and Dev.*, vol. 2, 166–168; 1958.
[5] C. E. Shannon and W. Weaver, "The Mathematical Theory of Communi tion," University of Illinois Press, Urbana, Ill.; 1959.

Abstracts of Current Computer Literature

(THROUGH APRIL, 1960)

These abstracts and the associated subject and author indexes were prepared on a commercial basis under the direction of Dr. Geoffrey Knight, Jr., who also publishes the abstract journal "Semiconductor Electronics." Local volunteer support of this endeavor has been furnished by Messrs. P. R. Bagley and R. P. Mayer of The Mitre Corporation, and F. E. Heart of Lincoln Laboratory, M.I.T.

Additional copies of these abstracts are available from IRE Headquarters, 1 East 79th St., New York 21, N. Y., at $1.00 per copy, or $3.50 for the set of four to be published in 1960.

—*The Editor.*

A-1: EQUIPMENT—THEORETICAL DESIGN

845

Man-Computer Symbiosis, by J. C. R. Licklider (Bolt, Beranek and Newman, Inc.); IRE TRANS. ON HUMAN FACTORS IN ELECTRONICS, vol. HFE-1, pp. 4–11; March, 1960.

Man-computer symbiosis, an expected development in cooperative interaction between men and electronic computers, will involve very close coupling between the human and electronic members of the partnership. The main aims are 1) to let computers facilitate formulative thinking as they now facilitate the solution of formulated problems, and 2) to enable men and computers to cooperate in making decisions and controlling complex situations without inflexible dependence on predetermined programs. In the anticipated symbiotic partnership, men will set the goals, formulate the hypotheses, determine the criteria, and perform the evaluations. Computing machines will do the routinizable work that must be done to prepare the way for insights and decisions in technical and scientific thinking. Preliminary analyses indicate that the symbiotic partnership will perform intellectual operations much more effectively than man alone can perform them. Prerequisites for the achievement of the effective, cooperative association include developments in computer time sharing, in memory components, in memory organization, in programming languages, and in input and output equipment.

846

The Operator Synthesis of Algorithmic Systems, by A. D. Zakrevskii; *Automation Express*, vol. 2, pp. 26–27; February, 1960.

The special features of a sequential conversion of information are studied, and the requirements for automatic information converters are determined. A method for synthesizing digital automatic devices is proposed. The method provides a formal transition from the operation conditions specified in the form of an algorithmic expansion of the conversion operator to the structure of the automatic device.

847

Mathematical Approach to Hybrid Computing, by G. Birkel, Jr., (Radiation, Inc.); *Proc. 1959 Natl. Symp. on Space Electronics and Telemetry*, pp. 2.1-1–2.1-7; September 28–30, 1959.

Simplification of sampled data reductions and control function problems by means of hybrid (analog and digital) computation techniques is discussed. The techniques are inherently compatible with usual equation formats. The operational laws are largely determined by linear transformation or mappings. A finite algebraic field is defined by the system. Floating-point arithmetic establishes a simple yet very flexible information format. A coding mesh related to a bounded reference subspace is defined with respect to a modulus or radix by a proportionality constant. A quantizing width defines the smallest possible mesh. Normalizing operations are performed on digital data prior to arithmetic operations. Normalizing techniques used are similar to the usual floating-point procedures. Provisions for underflow and overflow conditions are included. Techniques for analyzing and minimizing errors are especially simple in such a finite algebra.

848

Shift Registers with Logic Feedback and their Use as Computers and Encoding Devices (excerpts), by A. N. Radchenko and V. I. Filippov; *Automation Express*, vol. 2, pp. 29–31; February, 1960.

Methods for increasing the efficiency of computing and encoding devices which utilize shift registers are studied. The special feature of these devices is the fact that the shift register is a closed ring; the element which closes the ring is a logic network whose state is a function of the code introduced into the register. Methods for designing logic networks with feedback to produce computers or encoding devices with arbitrary capacity and methods for reading out information are presented.

849

Elapsed Time Computation, by H. W. Abbott and V. P. Mathis (General Electric Co.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 195–201; 1959.

A number of arithmetic operations using the amplitudes of independently variable electrical quantities are considered and sample calculations are performed. The variables are assumed to remain constant during the measurement interval or are appropriately sampled. Examples of semiconductor circuits employing the principles of elapsed-time computation are also given. These include systems having various combinations of analog and digital inputs and outputs. By interchanging the roles of reference voltage and input signals, the same circuits may be used for division, multiplication, squaring, and square-root operations. The use of this elapsed-time technique results in circuits that are simple and inexpensive, do not require precision components, and have an accuracy and dynamic range satisfactory for a wide range of applications.

850

On the Stability of Linear Algebraic Equation Solvers, by I. Cederbaum and A. Fuchs (Scientific Dept., Ministry of Defense, Israel); *Proc. Second Internatl. Analogue Computation Meetings*, pp. 174–178; September 1–6, 1958.

Conditions sufficient to assure the stability of analog computer set-ups for solving systems of linear equations are derived. The restrictions refer both to the characteristics of the operational amplifiers used and to the coefficient matrix of the equation systems. The accuracies of various methods which assure stability for all systems are compared. Finally, the design of the optimum amplifier and the adaptation of a conventional amplifier to this special task are discussed.

A-2: EQUIPMENT—COMPONENTS AND CIRCUITS

851

Domain Walls in Thin Ni-Fe Films, by S. Methfessel, S. Middelhoek, and H. Thomas (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 96–106; April, 1960.

Observations of domain walls in Ni-F films as a function of thickness demonstrat the strong influence of magnetic stray field on the wall structure, hence on the coercivit for wall motion. In order to reduce the stray field energy, the Bloch walls in films thicke than 1000 A are subdivided into section with alternating polarity, which are sepa rated by Bloch lines. In thinner films, th domain walls are of the Néel type. Th position of Bloch lines in such walls is in dicated by crosswalls. The motion of Bloc lines in an applied field can be observed par ticularly easily on scratches in negativ magnetostrictive material; such scratche display properties corresponding to Né walls. Crosswalls are also present at the end of domains and around holes in the film ma terial. A crosswall is distinguished fron ordinary domain walls by the continuou change of the angle of magnetization alon both sides of it.

852

Measurement of Magnetic-Field Attenua tion by Thin Super Conducting Films, b E. Erlbach, R. L. Garwin, and M. F Sarachik (IBM Corp.); *IBM J. Res. & Dev* vol. 4, pp. 107–115; April, 1960.

Measurement of the dependence of th field attenuation of thin superconductin films on temperature and superimposed d magnetic field with a sensitive RF bridge i discussed. Since theoretically the penetra tion depth λ can be derived from the attenu ation measurements, the experiment yields as a function of temperature and dc mag netic field. Changes in λ can be detected t an accuracy of ± 0.03 per cent. Preliminar data on the temperature dependence of λ fc lead are compared with the predictions c the Bardeen-Cooper-Schrieffer theory an are shown to be consistent with an energ gap between $4.9kT_c$ and $5.4kT_c$ at 0°K Detailed descriptions of the apparatus an of the preparation of the samples are giver

853

Magnetic Anisotropy in Single-Crystal Thi Films, by E. L. Boyd (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 116–129; April 1960.

Room-temperature measurement by torque method of the cubic crystalline anisc tropy constant, K_1, of thin single-crysta films of Ni, Fe, Ni-Fe, and Ni-Co, grown b vacuum deposition onto heated rock salt, i discussed. In the case of the Ni-Fe alloys, K was the same for thin films as for bulk ma terials of the same composition. The meas ured anisotropy in the Ni-Co films differ quantitatively but has the same qualitativ variation with composition as is reported fo bulk crystals. The results of one magneti annealing experiment on a 75 per cen Ni−25 per cent Fe film lends support to th short-range ordering model of uniaxial aniso tropy in alloys. Pure nickel films exhibit pronounced uniaxial anisotropy superim posed on the crystalline anisotropy, whic disappears after the film is removed from th substrate, indicating that its origin is in a anisotropic stress in the deposited film.

854

Angle-of-Incidence Anisotropy in Evaporate Nickel-Iron Films, by E. W. Pugh, E. L Boyd, and J. F. Freedman (IBM Corp.),

M J. Res. & Dev., vol. 4, pp. 163–172; ril, 1960.

Measurement by a torque method of the gnetic anisotropies of iron, nickel, and rmalloy films, evaporated onto glass subates at various incident angles and subnte temperatures, is reported. For all comsitions, the largest absolute value for the gnetic anisotropy occurs at the largest ident angle and lowest substrate temrature. A detailed calculation of the sotropy resulting from a [111] fiber axis ls to agree with the experimental results her in order of magnitude or in direction the easy axis. The change in the magnetic sotropies of films after removal from subates is small enough that macroscopic ess cannot be the source of the anisotropy. lifference in electrical resistance parallel H perpendicular to a direction defined by vapor stream during deposition is found vary qualitatively very much like the gnetic anisotropy, with both film comsition and incident angle. It is concluded t deposition at an angle of incidence proces an anisotropy in structural imperctions, which is interpreted in terms of ape and surface magnetic anisotropies as ll as magnetostrictive effects.

5

perconducting Tin Films of Low Residual sistivity, by G. J. Kahan, R. B. DeLano, , A. E. Brennemann, and R. T. C. Tsui BM Corp.); *IBM J. Res. & Dev.*, vol. 4, 173–183; April, 1960.

The production of evaporated tin films low residual resistivity by the use of very gh deposition rates in a conventional cuum system is reported. The substrates re cooled with liquid nitrogen. After the n edges are removed by mechanical mming or chemical etching, these films ow sharp magnetic and temperature nsitions from the superconducting to the rmal state, a critical field-temperature aracteristic which is close to a modified ver-n of the London theory, a transition mperature very close to the value of bulk , and a reversable resistance-critical curit characteristic. These characteristics are mpared with those of films deposited on bstrates at room temperature using low position rates. Evidence indicates that the ge effect in the temperature transition of ns is caused by a concentration of impurirs in the edges. The low-temperature mean e path, rather than the resistivity ratio, suggested as a figure of merit for estimatg film purity because the size effect limits e resistivity ratio for thin films.

6

n the Influence of Aggregation on the agnetic Phase Transition of Evaporated perconducting Thin Films, by M. E. hrndt, R. H. Blumberg, and G. R. Giedd BM Corp.); *IBM J. Res. & Dev.*, vol. 4, . 184–188; April, 1960.

An investigation of the magnetic phase nsition of thin, superconducting Sn films described. In evaporated films, because of e sloping edges, broad magnetic field nsitions are generally found. Such "pembra" effects can be eliminated by raising e temperature of the substrate during aporation. The lack of penumbra effect is e to the aggregation of the film. The transition curves of such films display hysteresis.

857

Magnetic Fields of Square-Loop Thin Films of Oblate Spheroidal Geometry, by H. Chang (Res. Lab., IBM Corp.,) and A. G. Milnes (Carnegie Inst. Tech.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 458–464; December, 1959.

Thin films of Ni-Fe alloy may be prepared to be anisotropic and exhibit square-loop M-H characteristics. In films that are single-domained with flux changes involving only rotation of intrinsic magnetization controlled by cross-magnetization fields, very fast switching action can be obtained for storage and logic functions. Problems of coupling to the flux changes and interaction in an array of such films require study of the magnetic-field distribution. In the treatment given, a circular, single-domain, thin film is represented by a very flat oblate spheroid. The field distribution outside the spheroid is found by assuming that the magnetic properties are characterized by an intrinsic magnetization M which is constant in magnitude but varies in direction depending on field and energy considerations. The field distribution is calculated for a typical film with diameter-to-thickness ratio of 10^5. From regions over which field changes are most significant, conclusions are drawn as to the proper size of sensing loops and spacing to avoid interaction during switching in film arrays.

858

Relaxation Times in Lead Film, Superconductive, Storage Elements, by R. F. Broom and O. Simpson (Services Electronics Res. Lab.); *Brit. J. Appl. Phys.*, vol. 11, pp. 78–80; February, 1960.

An important factor in the performance of any thin-film superconductive switching device is the speed with which superconductivity is restored after the film is driven into the normal conducting state. An experiment which measures the critical current of a lead-film Crowe cell during the first microsecond after switching is described. The minimum writing time of such storage cells should be equal to the time required for the critical current to recover to one-half of its initial value. Good correlation between the recovery times and the writing times has been found for Crowe cells deposited on various substrates. Cells deposited on mica or saphire recovered in 50 mμs, while those on glass required approximately three times as long. Measurements of the critical current as a function of temperature have also been made, and these are used to derive cooling curves during the recovery phase. The cooling curves are not related to the thermal conductivities of the substrates in any simple way, probably because the rate of cooling is determined primarily by the thermal resistance between film and substrate.

859

Nanosecond Switching in Thin Magnetic Films, by W. Dietrich, W. E. Proebster, and P. Wolf (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 189–196; April, 1960.

A special pulse equipment including a pulse-sampling oscilloscope with an over-all response time of 0.35 nanosecond (10^{-9} sec) for observing the nanosecond flux change in thin permalloy films is described. Film switching signals as short as 1 nanosecond have been obtained and are discussed with respect to the underlying processes. Inverse switching time vs driving-field curves, plotted for films of different thicknesses, show that thinner films switch faster than thicker ones. The slopes of these curves have characteristic values in the nanosecond region of about 10^8 per oersted-second. Coherent rotation and oscillation of the magnetization have been clearly detected by picking up the flux change transverse to the driving field.

860

High Frequency Magnetic Film Parametrons for Computer Logic, by A. V. Pohm, A. A. Read, R. M. Stewart, Jr., and R. F. Schauer (Iowa State Univ. of Sci. and Tech.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 202–214; 1959.

The construction of high-frequency magnetic-film parametrons (phase-locked subharmonic oscillators) using time-variable inductors made from 6×10^{-5} cm thick 80-20 permalloy films is described. The pump field was applied parallel to the rest direction of magnetization, while the signal field was applied perpendicular to it. Measurements of the transient response, frequency range, power consumption, and saturation characteristics were made using about a 14.5-mc pump frequency. Two- and three-state operations were observed for a single-bias condition; four- and five-state operations were observed when both bias conditions were allowed. The dynamic behavior of magnetic films has been analyzed in terms of a modified Landau-Lifshitz equation, and the parametron threshold and transient and saturation characteristics have been analyzed in terms of a modified Hill's equation. Calculations show that operation above 100 mc is possible using permalloy films.

861

Superconducting Circuits, by D. R. Young (IBM Corp.); *Progress in Cryogenics* (Academic Press), vol. 1, pp. 1–31; 1959.

Following a brief introduction to the phenomenon of superconductivity, several superconductive devices and circuits are reviewed. The cyrotron and several circuits which utilize the device, including a comparison circuit, logic circuits, a binary adder, and a latching circuit, are described. Persistent current memory devices and circuits are considered, and some predictions of future developments in superconductive devices are made.

862

The Variation of Cryotron Current Amplification Factor with Temperature, by A. E. Brennemann (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, p. 197(L); April, 1960.

Measurements of the variation of the current amplification factor of thin-film cryotrons with temperature, as the temperature is lowered from the critical temperature of the gate, are reported. The amplification factor is zero at the critical temperature and increases rapidly as the temperature is lowered below the critical temperature. The amplification factors measured were less

than one-tenth the values predicted by the ratio of the gate-film width to the control-film width when the helium-bath temperature was near the critical temperature of the gate. It is concluded that the ratio of the penetration depth to film thickness is a significant variable and that this places a lower limit on the film thickness that can be used in practice.

863

A New Storage Element Suitable for Large-Sized Memory Arrays—The Twistor, by A. H. Bobeck (Bell Telephone Labs., Inc.); *Bell. Sys. Tech. J.*, vol. 36, pp. 1319–1340; November, 1957.

The basic theory of the twistor device is developed. The effect of applied torsion shifts the preferred direction of magnetization in the wire into a helical path inclined at 45° to the axis. Coincident circular and longitudinal magnetic fields insert information into the wire. The wire itself may be used for readout. The possibility of applying weaving techniques to twistor arrays makes their application economically attractive.

864

Electrodeposited Twistor and Bit Wire Components, by S. J. Schwartz (Natl. Cash Register Co.) and J. S. Sallo (Minneapolis Honeywell Regulator Co.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 465–469; December, 1959.

The production of magnetic storage elements through electrodeposition of ferromagnetic materials on wire is discussed. One form, known as a twistor, has magnetic properties suitable for memory application when it is placed under torsional strain. A new device called a bit wire differs in that it does not require external stressing. The materials possess the desirable temperature stability usually associated with ferromagnetic metals and exhibit a high signal-to-noise ratio. Both linear-selection and coincident-current memory arrays have been constructed with bit wire and plated twistors. The switching characteristics and drive requirements are similar for both materials. Both devices are packaged, since undesired strains can change their properties. This problem has been minimized by plating the bit-wire material on semirigid wire or tubing. The tubular structure offers other advantages, since additional sense, drive, or inhibit wiring may be threaded through the tube.

865

Integrated Magnetic Circuits for Synchronous Sequential Logic Machines, by U. F. Gianola (Bell Telephone Labs., Inc.); *Bell Sys. Tech. J.*, vol. 39, pp. 295–332; March, 1960.

The possibility of building logical systems that use a minimum of non-magnetic components is examined. Except for the provision of clock-pulse sources, fully integrated magnetic machines are feasible in principle. Suitable circuits must contain provision for gain, memory, and unilateral transmission of data. These requirements can be met by taking advantage of the threshold characteristics of ferromagnetic materials that have a rectangular hysteresis loop, and two approaches are selected for consideration. In the first, a binary digit is represented by the remanent state of magnetization of a ferrite core. Upon the application of clock pulses its state can be transferred to adjacent cores by means of electrical interconnections. In the second approach, a binary digit is represented by a discrete flux pattern in a continuous flux conductor. These patterns can be propagated in a step-by-step process through the flux conductor by means of clock pulses. Examples of experimental synchronous sequential circuits using commercially available multiapertured cores are given, and their capabilities, limitations, and organization are discussed.

866

Ferroresonant Systems of Circuit Logic, by J. G. Santesmases, M. Alique, and J. L. Lloret (Instituto de Electricidad y Automatica, Madrid); *Proc. IEE*, vol. 107, pt. B, pp. 190–198; March, 1960.

Following a description of the logical behavior of a basic ferroresonant circuit, a procedure for obtaining the AND and OR fundamental circuits with ferroresonant elements is presented. The possibility of coupling these fundamental circuits allows the development of a ferroresonant system of circuit logic. A ferroresonant inhibit circuit and the simplification it permits in the logical system are studied and the results obtained are described.

867

The Use of Silicon Diodes in D.C. Modulators and Their Applications to Drift Correctors for Computing Amplifiers, by T. Glucharoff and C. P. Gilbert (Univ. of New South Wales); *Proc. IEE*, vol. 107, pt. C, pp. 82–90; March, 1960.

The basic computing element of an electronic analog computer is the high-gain dc amplifier, but in order to overcome its inherent drift, some form of auxiliary drift-correcting amplifier is frequently used. A silicon diode modulator for use in such drift correctors is described, and it is shown that the zero stability which can be achieved is comparable with that given by the conventional relay modulator. It is also shown that the use of the diode circuit results in a number of improvements in the over-all drift-corrector performance, such as a higher-frequency response and practically unlimited life. The design of such a drift corrector for use with a given dc amplifier is described in detail, and the resulting performance is evaluated.

868

A Compensation Technique for Reduction of Performance Errors of Operational Amplifiers, by K. P. P. Nambiar and A. R. Boothroyd (Univ. of London); *Proc. IEE*, vol. 106, pt. B, suppl. no. 15, pp. 496–504; 1959.

A simple compensation technique, previously employed to improve the sweep linearity of bootstrap sweep generators, is investigated as a means of reducing the performance errors of operational amplifiers. It is shown that such compensation is capable of quite general application but is of most value in the case of transistor amplifier circuits, where the active element may be regarded as a current amplifier. Thus, multiple-input transistor operational amplifiers may be improved by compensation, whereas i the vacuum-tube amplifier case the tech nique is restricted to single-input circuit Simple forms of compensating circuits ar derived for summing, integrating, and di ferentiating amplifiers; correction for th fall of gain of the active element at hig frequencies is also included. The main result are illustrated by practical examples i which the active element is a single commor emitter stage.

869

Transistor Pulse Circuits for 160-MC Cloc Rates, by W. J. Giguere, J. H. Jamison, an J. C. Noll (Bell Telephone Labs, Inc.); IR TRANS. ON ELECTRONIC COMPUTERS, vo EC-8, pp. 432–438; December, 1959.

Two methods of regenerating 6.25-mμse pulses at a 160-mc bit rate are discussed. Th first consists of dc level restoration for recog nition of the signal and constant-current co incident circuitry for reconstruction of th pulses. The second consists of operating o changes in the signal for pulse recognitio and the use of a bistable circuit for pulse re construction; timing is obtained by constant-current coincidence gate. Paralle to-serial multiplexing techniques to combin 16 parallel 10-mc clock-rate signals into 160-mc clock-rate pulse train are then con sidered. The 16 synchronous signals ar applied to 16 AND gates along with a 10-m narrow-gate pulse. The space separation o the resulting regenerated and timed AN gate output pulses is converted to time sepa ration with only a small amount of signa loss, by injecting the pulses at 16 equall separated points on a broad-band delay lin Methods to reduce spurious responses result ing from multiple reflections on the dela line have been developed. The current mod transistor AND gates are suitable fo AND/OR functions for individual 4-mμse logic. The multiplexer may also be used a test equipment to generate repetitive 16-bi binary words with a 10-mc frame rate.

870

Ripple-Type Time-Delay Networks Usin Elliptic Functions, by J. R. Kiseda an D. J. Ford (Univ. of Pittsburgh); *Commun and Electronics*, no. 46 (*Trans. AIEE*, pt. vol. 78), pp. 996–1002; January, 1960.

A method of designing approximate time delay simulation networks in the frequenc domain is presented. The method utilizes a expansion of the steady-state sinusoida transfer function of an ideal time-delay de vice into the quotient of two polynomials i ωT_d. By taking a finite number of terms o the expansion, an approximation to th ideal time-delay device is obtained. If th corresponding coefficients in the numerato and denominator are set equal (except fo the signs of some terms), the quotient wi possess a constant unity-gain for all positiv frequencies which is characteristic of all-pas structures and a phase characteristic whic may be adjusted at will. By setting th group-delay equal to a desired ripple-typ function, it is possible to cause the phas characteristic to ripple about the idea linear-phase curve. The details of the de velopment are illustrated for an elliptic-typ ripple function in second- and fourth-orde transfer-function configurations.

A-3: EQUIPMENT—SUBSYSTEMS

Decimal Adder Using a Stored Addition ble, by M. A. Maclean and D. Aspinall niv. of Manchester); *Proc. IEE*, vol. 105, B, pp. 129–135; March, 1958.

A serial decimal adder which accepts mbers in binary coded form and utilizes a red table is described. The digits 0 ough 9 are encoded in terms of their idues modulo 5 and 2, thus saving on rage space. Square-loop magnetic cores used for all logical functions and junction nsistors for pulse amplification.

2

High-Speed Multiplication Process for gital Computers, by F. Gurzi (Litton dustries); *Commun. Assoc. for Computing uch.*, vol. 3, pp. 241–245; April, 1960.

A method of high-speed multiplication sed on the Booth and Booth method is scribed. The product of two n-digit mbers is yielded in between $n/2$ and $n/3$ -periods. The method depends on exam- ng several successive digits of the multi- er and making provision for multiple fts. The increased speed requires addi- nal diode logic and instruction circuits d a complex counter.

3

e Design of a Large Electrostatic Mem- y, by M. Graham, G. L. Miller, H. R. te, and R. Spinrad (Brookhaven Natl. b.); IRE TRANS. ON ELECTRONIC COM- TERS, vol. EC-8, pp. 479–485; December, 59.

A large, high-speed, random-access emory for the Brookhaven "Merlin" digi- computer is described. This system em- oys barrier-grid electrostatic-storage tubes a novel configuration yielding improved iability. Basic design considerations are esented, together with a description of rcuitry and performance.

4

illimicrosecond Diode Capacitor Memory, M. M. Kaufman (RCA); *Proc. Natl. ectronics Conf.*, vol. 15, pp. 215–225; 1959.

The 1953 National Bureau of Standards ode capacitor memory of 10,000 bits with 10-μsec cycle time used diodes of the junc- n type which have a basic speed limitation cause of minority carrier storage and dif- sion time. It has been shown, using faster odes, that the cycle time for a diode pacitor memory can be reduced to 10 sec. The diode capacitor storage tech- que has been studied, and a prototype emory has been built to evaluate the dif- ulties in reducing the cycle time to this vel. A theoretical analysis considering the orst conditions for operating such a emory has allowed tabulation of its ulti- ate capabilities.

5

pandable Random Access Memories, by E. Lund and D. R. Faulis (Burroughs rp.); *Electronics*, vol. 33, pp. 164–166; arch 11, 1960.

The transistor circuits employed in the emory of the Burroughs B-251 Visible ecord Computer are presented and their eration is described. The computer emory can be expanded by means of plug- in memory packages. Additional word switches (bilateral switches) are required for the added memory packages. The linear select random-access configuration of the magnetic core memory permits operation over the temperature range 15°–55°C without critical components or currents. Memory access time is approximately 10 μs.

876

Diode-Steered Magnetic-Core Memory, by A. Melmed and R. Shevlin (New York Univ.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 474–478; December, 1959.

Techniques which take advantage of word arrangement to make possible large high-speed magnetic-core memories at moderate cost are described. Economy is obtained by means of a two-coordinate selection system using diffused junction rectifiers as steering diodes. By taking advantage of the relatively slow recovery time of these rectifiers, automatic rewrite selection is obtained in a similar sense to that provided by a biased switch core. The familiar "inhibit" line is eliminated, reducing the memory array to a two-wire configuration. And finally, the customary core-array geometry is rearranged to facilitate winding the digit wire as a balanced twisted-pair transmission line, thereby eliminating the effect of post-write disturb.

877

A Small High-Speed Transistor and Ferrite-Core Memory System, by W. L. Shafer, Jr., W. N. Toy, and H. F. Priebe, Jr. (Bell Telephone Labs., Inc.); *Commun. and Electronics*, no. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 763–769, January, 1960; *Electrical Engrg.*, vol. 79, pp. 212–217, March, 1960.

The design and operation of a 400-bit ferrite core memory for use in a time-division electronic switching system are described. A cycling binary counter establishes sequential access to the twenty rows (twenty twenty-bit words) of the memory. The readout is blocked except when opened by a strobe pulse during the read period, to prevent partial switching caused by noise from the vertical-write pulse. Synchronization is by external clock; the read cycle takes 5 μsec per word, or 100 μsec to cycle through the memory. Operation has been checked for supplying voltage and temperature variation with favorable results reported.

878

A 32,000-Word Magnetic-Core Memory, by E. Foss and R. S. Partridge (IBM Corp.); *IBM J. Res. & Dev.*, vol. 1, pp. 103–109; April, 1957.

The development of the IBM 738 magnetic core storage unit is summarized. Engineering problems such as the electrical and mechanical arrangements for packaging more than one million cores and their circuits are discussed. The driver circuits and sense amplifiers used in the system are described.

879

A Magnetic Matrix Switch and Its Incorporation into a Coincident Current Memory, by K. H. Olsen (Mass. Inst. Tech.); *U. S. Govt. Res. Repts.*, vol. 33, p. 183(A), February 12, 1960; PB 144 069 (order from LC mi $5.70, ph $16.80).

A multiposition switch constructed from magnetic cores which is capable of handling pulses shorter than one microsecond is described. Windings on the magnetic cores, when matrix-connected, control selection of the switch output; they can be excited with either direct current or pulses. The switch is capable of transmitting power efficiently, and the magnetic cores from which it is made are inexpensive and rugged and promise reliability and long life. Two such switches pulse the 16 coordinate rows and the 16 coordinate columns of a coincident-current magnetic-core memory. The complete cycle-time of the memory, including the switch setup time, reading of information, and rewriting of information, is less than four microseconds. Design of the magnetic matrix switch is facilitated by an equivalent-circuit technique.

880

Nondestructive Readout of Metallic-Tape Computer Cores, by L. M. Lambert (Ford Motor Co.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 470–474; December, 1959.

Nondestructive readout of metallic-tape memory cores by the application of a magnetomotive force spatially in quadrature to the direction of remanent flux is discussed. A simple method of fabrication is proposed, and empirical data for the design of the nondestructive readout systems are obtained. An experimental shift register has been built to test the method. The nature of the system permits high-speed low-current-level operation in either digital or analog applications.

881

EDVAC Synchronous Magnetic Drum, by C. H. Wallin and J. G. Gregory (Aberdeen Proving Ground); *U. S. Govt. Res. Repts.*, vol. 33, p. 293(A), March 18, 1960; PB 144 085 (order from LC mi $2.70, ph $4.80).

The electrical, logical, operational, and servicing features of the EDVAC synchronous magnetic-drum storage system are described. The technique used to synchronize drum rotation with the EDVAC system, the method of transferring information to and from the drum, and the necessary controls for controlling the flow of information are completely described. Schematic, logical, and mechanical drawings are included.

882

A Magnetic Drum with a One Megabit Storage, by R. R. Schaffer (IBM Corp.); *Electronic Industries*, vol. 19, pp. 114–117; March, 1960.

A prototype magnetic drum memory which utilizes a standard IBM 650 drum assembly and has eight times the storage capacity of the standard memory with the same access time is described. The increase in storage capacity results from the use of high resolution magnetic drum heads and the same access time from the use of high-speed transistor circuits. These circuits, the drum, and the drum head are described.

883

High Speed Track Selection for a Magnetic Drum Store, by A. D. Booth (Birkbeck College); *Electronic Engrg.*, vol. 32, pp. 209–211; April, 1960.

Following a short account of the methods

which have been used for the selection of tracks on a magnetic drum store and a discussion of two conventional transistor head switches, a new head switch which uses a simple symmetrical transistor and which has the advantage of not injecting a large transient into head and amplifier at the instant of switching is described.

884
A Magnetic-Drum Store for Analog-Computing, by J. L. Douce and J. C. West (Queen's Univ., Belfast); *Proc. IEE*, vol. 105, pt. B, pp. 577–580; November, 1958.

The use of a comventional magnetic drum in analog computation is described. The drum supplies a large storage capacity with relatively short access time. Several of the important facilities obtained by this technique, such as flexible function generation and time delay, and ease of multiplication, are discussed.

885
Ferroelectrics for Digital Information Storage and Switching, by D. A. Buck (Mass. Inst. Tech.); *U. S. Govt. Res. Repts.*, vol. 33, p. 183 (A), February 12, 1960; PB 144 326 (order from LC mi $4.50, ph $12.30).

Recently discovered materials, known as ferroelectrics, within which exist domains of permanent electric dipoles, can be used to advantage in many electronic applications where ferromagnetic materials are currently used, often in circuits which are the duals of those of their ferromagnetic counterparts. Ferroelectrics can be made in the form of single crystals or rugged ceramics. Digital information can be stored in a matrix of ferroelectric condensers, and an efficient method of storage-element selection is available in the form of a two-coordinate, coincident-voltage scheme. The matrix can be made on a thin ferroelectric sheet by painting the coordinate rows on one side and the coordinate columns on the other. The information can be taken from the matrix via a simple mixing transformer.

886
A High-Speed, Electronic Analog-to-Digital Encoder, by R. C. Platzek, H. F. Lewis, and J. J. Mielke (North American Aviation, Inc.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 182–194; 1959.

A high-speed, semiconductor, bipolar analog voltage encoder with fourteen-bit capacity which accepts and continuously converts voltages that are static or varying at rates not exceeding 2500 volts per second is described. The output is a binary-coded decimal equivalent of the input voltage presented for parallel readout. A general description based on a block diagram representation of the encoder is presented, including pertinent characteristics and performance specifications. The analysis of the encoder emphasizes the nature of the system error signals and the techniques used to achieve stable performance. Means of extending the versatility of the device, inherent limitations, and quantitative performance are also discussed.

887
Magnetic Amplifier Binary-to-Analog Conversion, by I. Danylchuk and D. Katz (Bell Telephone Labs, Inc.); *Commun. and Electronics*, no. 46 (*Trans. A IEE*, pt. I, vol. 78), pp. 909–912; January, 1960.

Two magnetic amplifier binary-to-analog converter circuits are described. A five-digit binary-to-analog converter utilizes a saturable reactor with five signal windings. The number of turns in each control winding is weighted according to the significance of the binary digit with which it is associated. A 10-digit binary-to-analog converter utilizes three saturable reactors since it is not practical to put ten control windings on the same reactor. The three saturable reactors are arranged so that their output voltages are added to obtain the analog of the 10-digit binary input. The final stage of the 10-digit converter, a self-balancing magnetic amplifier with a voltage gain of four, increases the 0 to 25.575 volts average output of the first stage to the 102.3 volts average needed to drive a servomagnetic amplifier and to position a stylus which plots the analog values. The converter is accurate to better than one part in a thousand but is limited to situations where speed of response is not an important factor.

888
Digitalized Pickoff Display Converter, by F. R. Fluhr (Naval Res. Lab.); *U. S. Govt. Res. Repts.*, vol. 33, p. 184(A), February 12, 1960; PB 138 311 (order from LC mi $1.80, ph $1.80).

The use of digital methods in naval data-handling systems is discussed. One means by which an operator can insert and correct target track data as displayed on a radar plan-position indicator (PPI) is through the use of the Pickoff Display Converter (PDC). A digitalized PDC can convert an operator's positioning of an inserted marker displayed on the PPI with the radar video into the digit values representing the marker coordinates. The positioning of the marker is accomplished by positioning a probe on the surface of a conducting-glass PPI overlay. When the operator lifts the probe, the marker coordinate values are transferred to the main computer. The proposed digitalized PDC can be made to operate so that the probe will move the PPI marker in a direct 1:1 relationship or in a vernier-differential relationship.

889
Shift Register Transistors, by J. T. Wallmark (RCA); *U. S. Govt. Res. Repts.*, vol. 33, p. 183(A), February 12, 1960; PB 143 634 (order from LC mi $2.40, ph $3.30).

The concept of integrated electronics, *i.e.*, the idea of "molding" or integrating several component functions, active as well as passive, into one piece of material, is discussed. In the case of semiconductors, one might talk of integrated semiconductor circuits or devices of which the shift register is an example. By application of the integrated electronics approach to other semiconductor structures, a whole new class of integrated semiconductor devices using unipolar transistors has been developed. The unipolar transistor, although inferior to the conventional bipolar transistor in high-frequency response and power capabilities, may offer advantages in noise and radiation tolerance under certain conditions. The integrated device approach can be extended also to tuned circuit functions, such as radi and communication circuits.

890
An Eight Digit Word Generator, by P. L Owen and T. R. H. Sizer (Royal Aircra Establishment); *Electronic Engrg.*, vol. 3 pp. 134–139, March, 1960; pp. 212–21 April, 1960.

A binary word generator which utilize surface barrier transistors and direct couple logic and which was built as a piece of te equipment for the subsequent developme of digital computer elements is described. brief explanation of serial and parallel oper tion leading to the conception of serial wo representation, and thus to the need for word generator as a basic tool in this kind work, is given. The direct coupled tec nique is described and the limiting cond tions of the technique are pointed out. Th use of a transistor as a logical switch is di cussed, and it is shown that in the case of *p-n-p* device there is a relation between th speed of operation, the hole storage in th base region, and the degree of saturation. is emphasized, however, that this relatio ship is discussed only far enough to sho that a fast switching speed is possible wit out control of saturation conditions provid certain types of transistors are used.

891
Rotating Cylinder Function Generator, F. V. Cairns (Natl. Res. Council, Ottawa *Rev. Sci. Instr.*, vol. 31, pp. 454–455; Apr 1960.

A rotating-cylinder analog comput function generator is described and cor pared with a previously described rotatin disk function generator (see abstract 431 The principle of operation of each generat is the same, but in the rotating-cylind generator the function to be generated plotted without any transformation, exce scaling, and a number of outputs, each repr senting the desired function with a differe delay, may be obtained simultaneousl Sources of error in the generator are di cussed and techniques for reducing them a outlined.

892
Simple Analog-Computer Sawtooth Ge erator, by R. A. Eubanks (Borg-Warn Res. Center); *Instruments and Control Sy tems*, vol. 33, p. 251; February, 1960.

An analog computer sawtooth functi generator which is stable in both peak amp tude and period and does not require an e ternal frequency determining circuit, co tains few components, and in which there no interaction between the frequency contr potentiometer and the amplitude contr potentiometer, is briefly described. T generator is compatible with all operation computers known to the author.

893
Twelve Digit Binary Encoder, by R. Smith (ACF Industries, Inc.); *U. S. Gov Res. Repts.*, vol. 33, p. 293 (A), March 1 1960; PB 138 092 (order from LC mi $3.3 ph $7.80).

An analysis of the development and co struction of a 12-digit binary encoder whi converts dc analog voltages to correspondi binary numbers is presented. The devi

)duces binary digital numbers consisting 11 bits and a sign bit at the rate of 500 nplete codes per second. The encoding e is determined by the frequency of an ernal start pulse and can vary from zero the maximum of 500 codes per second. e analog input range is −50 v to +50 v, ile the binary parallel output range exds from all zeros at −50 v to all ones at 0 v. The five phases of the project (sysns study and design, circuit design and t, prototype construction and test, final del construction and test, and the inuction manual and final report) are dissed. The problems encountered are nted out and their solutions are given. otographs of the final model are included h drawings and specifications, and it is licated that the unit can be reproduced ily and economically. The feasibility of nsistorizing the encoder is discussed.

4
e Design of the Control Unit of an Elecnic Digital Computer, by M. V. Wilkes, Renwick, and D. J. Wheeler (Cambridge iv.); *Proc. IEE*, vol. 105, pt. B, pp. 121–8; March, 1958.

The logical design and practical implentation of the control unit for a digital mputer are discussed. A systematic and xible design using two major groups of stems is described. In the first, the order de is determined by the arrangement of odes in a matrix and in the second by the propriate threading of wires through a rite core matrix.

5
n the Error of a Linear Interpolator for a gital Program Control System, by V. P. aribskii; *Automation Express*, vol. 2, p. 23; bruary, 1960.

The principle of operation of a linear gital interpolator is described, and a eoretical study of the interpolation error performed. The general expression for the ror is derived, and the maximum possible solute error is estimated.

6
Second-Order Interpolator for Digital rogram Control Systems (excerpts), by P. Karibskii; *Automation Express*, vol. 2, p. 32–34; January, 1960.

The block diagram and operational gorithm for an interpolator which controls e movement of a cutting tool between two ference points on a parabola are described.

7
Real-Time Simulation System for Use ith an Analog Simulator, by M. Palevsky Packard Bell Computer Corp.); *Proc. econd Internatl. Analogue Computation leetings*, pp. 400–402; September 1–6, 1958.

Some newly developed digital devices hich can be employed with analog comuters are described. These devices include n extremely high speed incremental comuter for computing nonlinear analytic funcons, a function generator that employs hotographic techniques for storage, and a 01 per cent analog-to-digital and digitalo-analog converter. The converter also erforms multiplication and division within he conversion process.

898
An Improvement to the Electron-Trajectory Tracer, by J. Vine (Siemens Edison Swan, Ltd.) and R. T. Taylor (Associated Electrical Industries, Ltd.); *Proc. IEE*, vol. 107, pt. B, pp. 181–184; March, 1960.

To increase the accuracy of the trajectory tracer (see abstract 783) improved methods of field determination on the resistance network have been investigated. One of these—an interpolation system applicable to axially symmetric fields—is described. This system has been constructed and some results obtained with it for trajectories through an electron lens are given. These are compared with corresponding results obtained without the interpolation device and with results obtained by other methods. The interpolation system provides significantly increased accuracy for this particular type of problem with little extra complication in the operation of the trajectory plotter.

899
An Error-Detection System for 5-Unit-Code Teletypewriter Transmission, by P. H. Barry (Teletype Corp.) and A. L. Whitman (Bell Telephone Labs., Inc.); *Commun. and Electronics*, no. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 916–921; January, 1960.

A system for detecting errors in data transmitted to and from a computer by means of five-unit telegraph code is described. The transmission is from punched paper tape in a transmitter-distributor. After each checking block of text (*i.e.*, a type line of about 72 characters or a portion of a line terminated by a carriage return signal) is transmitted, a check character unique to its checking block is generated and transmitted to the receiving station. A new check character is generated at the receiving end from the received text by the same process as at the sending end and the character is compared with the transmitted character. Disagreement between the two indicates that an error exists in the preceding line of text. The system is not automatic, *i.e.*, an operator must request retransmission of the portion of the text in error, and applies only to transmission errors. Techniques for detecting operator errors in preparing the punched tape and errors resulting from the incorrect operation of the transmitter-distributor are described. The five-level checking scheme gives a theoretical probability of an undetected error in a checking block of about one in every 125 million characters.

A-4: EQUIPMENT—DIGITAL COMPUTERS

900
Microminiaturizing a Space Vehicle Computer, by E. Keonjian (American Bosch Arma Corp.); *Electronics*, vol. 33, pp. 95–98; April 29, 1960.

The fabrication of digital computers with high parts density is discussed. Three versions of a full adder which utilize the two-dimensional microminiaturization technique are described. Individual functional circuits are produced on a thin, insulating substrate by means of printed resistors, barium titanate capacitors, and unencapsulated semiconductor diodes and transistors. The functional circuits are then interconnected by means of wires between the wafers (the wires also provide mechanical support), by means of a printed wire board, or by a flexible interconnection strip which is then folded like an accordion. Thin-film transfluxors about 0.1 inch in external diameter, and the wiring and packaging of a transfluxor storage matrix for a memory with about 30,000 bits, are briefly described.

A-5: EQUIPMENT—ANALOG COMPUTERS

901
The Simulation of Electron Kinetics in Semiconductors, by G. Brouwer, Jr. (Philips Res. Labs.); *Proc. Second Internatl. Analogue Computation Meetings*, pp. 135–138; September 1–6, 1958.

The analysis of the distribution of electrons and holes in semiconductors under excitation by light pulses leads to a set of rather complicated nonlinear differential equations containing numerous unknown parameters. As the latter have to be determined by a trial and error method, it was found that an analog computer was most suitable for the problem. A special-purpose simulator designed for this purpose which contains eight multipliers, four integrators and a signal generator is described. The simulator is of the repetitive type, and the cycle is started with the zero setting of the integrators, followed by the insertion of the initial values. DC restorers are employed whenever the absolute value of the signal is of importance, as it is in the case of multiplication. A simple master clock synchronizes the various phases of the computation cycle. The time constants of the integrators are adjustable and are usually set on different time scales in one and the same problem. With the simulator it is possible to study the dynamics of photoconductivity, fluorescence and thermal stimulation in semiconductors and the dynamics of the spin system in a maser.

902
A Train Performance Computer, by E. Bradshaw, M. Wagstaff, and F. Cooke (Manchester College of Sci. and Tech.); *Proc. IEE*, vol. 105, pt. B, pp. 560–568; November, 1958.

An analog computer employing a 50-cps computing circuit which uses induction energy meters as integrators to evaluate locomotive performance is described. Automatic and continuous predictions of speeds, running times, energy consumption, and root-mean-square motor current are supplied by the computer. Typical studies of train performance are illustrated.

903
An Electronic Simulator for Processing Data on Extensive Atmospheric Showers of Cosmic Rays (complete), by G. V. Bogoslovskii and B. A. Khrenov (Moscow State Univ.); *Automation Express*, vol. 2, pp. 34–36; January, 1960.

An analog computer which solves the problem of finding 1) the most probable position of the axis of an extensive atmospheric shower and 2) the number of particles in a shower is described. The device simulates a mathematically accurate solution of the problem and yields the probability distribu-

tion with respect to the coordinates of the shower axis in the plane of observation and with respect to the number of particles in the shower. The accuracy of the solution is analyzed.

904
An Analogue Computer for Investigating the Directivity Characteristics of Complex Arrays of Unit Aerials, by G. Mitchell (P.O. Res. Sta.); *Post Office Electronics Engineers' J.*, vol. 52, pp. 246–250; January, 1960.

An analog computer which can compute automatically the directivity characteristics of an array of aerials which operates in high-frequency band and which consists of from 50 to 200 unit aerials, with the aerials arranged along from one to 16 diametral rows intersecting at a common point and with a maximum of 14 aerials in any one diametrial row, is described. The computer can also be used on a semi-automatic basis for dealing with larger or more complex arrays.

A-6: EQUIPMENT—DIGITAL-ANALOG COMPUTERS

905
High-Speed Hybrid Computers, by M. C. Burns (Radiation, Inc.); *Proc. 1959 Natl. Symp. on Space Electronics and Telemetry*, pp. 2.2-1–2.2-9; September 28–30, 1959.

High-speed real-time computation by means of a hybrid (analog and digital) computer is discussed. The hybrid utilizes both analog-to-digital and digital-to-analog converters to perform computations. A basic hybrid computer is described, and typical hybrid computations are presented.

906
A Digital-Analog Controller for Sampled Data Systems, by S. C. Bigelow (Columbia Univ.); *U. S. Govt. Res. Repts.*, vol. 33, pp. 293–294(A), March 18, 1960; PB 143 961 (order from LC mi $3.60, ph $9.30).

A practical digital controller for sampled-data control systems, which is a hybrid digital-analog computer programmed to solve the control equations, is described. The machine input and output signals are voltage analogs in the range of −50 to +50 volts. Arithmetic operations are performed using analog computer circuits, while storage is accomplished in digital storage registers. Analog-to-digital and digital-to-analog conversions are performed internally. The controller serves a twofold purpose by demonstrating the feasibility of applying the well-developed theory of sampled-data control systems to real processes, and by providing a useful tool for further study of such systems.

B-1: SYSTEMS—THEORETICAL DESIGN

907
Status of Sampled-Data Systems, by E. I. Jury (Univ. of California); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 769–777; January, 1960.

Procedures for analysis and methods of synthesis of sampled-data systems are briefly described. The present areas of research and some important problems in this field are indicated. The following items are discussed: 1) Methods of analysis of linear sampled systems, including the Z-transforms, frequency response, impulsive response, and difference-equation methods. 2) Procedures for design of sampled-data systems or continuous-control systems employing digital computers. Both time and frequency-domain methods are described. 3) Types of implementation of discrete and continuous compensation networks. 4) Sampled-data systems with finite pulse width and pulse-modulated feedback systems and methods for their analyses. 5) An experimental study of a simulated system on a specially built computer.

908
Extended Synthesis Techniques for Multipole Sampled-Data Control Systems, by E. B. Stear and C. T. Leondes (Univ. of California); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 299–309; 1959.

After a discussion of the shortcomings of existing techniques for the synthesis of multipole sampled-data control systems, a logical and efficient procedure is presented. It is assumed that the specifications on the system are stated in the time domain, which is a common situation. Furthermore, it is not assumed that the specifications are stated only at the sampling instants of the system, but rather at arbitrary and necessary instants of time. In addition, a lower bound is established for the sampling rate based on system requirements. This last exceedingly important aspect has received very little attention in the literature.

909
Multiple-Rate Sampled-Data Systems, by L. A. Gimpelson (Mass. Inst. Tech.); IRE Trans. on Automatic Control, vol. AC-5, pp. 30–37; January, 1960.

The characterization of multiple-rate sampled-data systems by the ordinary z transform of single-rate systems is shown. Single-rate sampling, or impulse modulation, of continuous signals is performed by an impulse modulator M; the sampled, or "starred," function is described by the z transform. In an analogous manner, a submultiple-rate modulator is introduced; its presence in a branch allows the pasage of every nth pulse, or a train of pulses at a submultiple rate; the nomenclature of single-rate systems is continued through the performance of submultiple-rate "starring" of discrete signals and discrete filters. Starred expressions can be rewritten as functions of the z transform in closed form. Techniques are shown for the reduction of discrete, and mixed continuous and discrete, systems via flow graphs, so that after the modulators are removed from the feedback loops, the analysis may proceed by standard methods. Representation of single- and submultiple-rate modulation in the s and z planes is used to demonstrate that submultiple-rate modulation of discrete signals is analogous to the impulse modulation of continuous signals.

910
The Minicard Interim Development Program (Eastman Kodak Co.); *U. S. Govt. Res. Repts.*, vol. 33, p. 184(A), February 12, 1960; PB 142 936 (order from LC mi $11.10, ph $42.60).

A serial-scan code-reader scheme is proposed and compared with the present parallel-scan code reader. Serial scan offers the following potential advantages: increased card code capacity, increased readout rate broader film-density tolerances, and broade card-positioning tolerances. It is propose that the serial code reader use a flying spo scanner with edge following and binary puls positioning modulation code. Block dia grams show how such a serial code reade might be developed. The questions of filn wear and of X-radiation are examined in de tail. The size and complexity of a serial-sca code reader are estimated.

B-2: SYSTEMS—DESCRIPTIONS

911
General Purpose Digital Computing Systems, by A. H. Freilich (Burroughs Corp.); *Electronic Industries*, vol. 19, No. 2, pp 70–75; February, 1960.

Following a discussion of the use o general-purpose digital computers in proces control applications, nine such computer are described and compared. Installations o process-control computers and general-pur pose digital computers which are on orde for process control applications are listed.

912
IBM Military Computer System, by F. S Morreale (Rome Air Dev. Center); *U. S Govt. Res. Repts.*, vol. 33, p. 294(A), Marc 18, 1960; PB 144 467 (order from LC m $2.40, ph $3.30).

The general-design characteristics of computer system developed by IBM to mee the data-processing requirements of th Semi-Automatic Ground Environmen (SAGE) and Strategic Air Command Con trol (SACCS) Systems is described. Th term "IBM Military Computer" is an IBM nomenclature. Air Force nomenclature fo the SAGE version is AN/FSQ7-A; th SACCS version has no Air Force nomencla ture. The major computer elements an typical peripheral equipments that make u the complete data-processing system are de scribed briefly.

913
An Analog and Digital Airborne Data Acquisition System, by D. H. Ellis and J. M Walter, Jr. (Radiation, Inc.); Proc. IRE pp. 713–724; April 1960.

A highly flexible analog and digital air borne data acquisition system is describe The acquired data are recorded on 1-inc tape. The format may be 14 tracks of analo or 7 tracks of analog with 16 tracks of digit data. Ampex AR-200 equipment is used o the analog subsystem. Complete analog sys tem reference data are recorded on one track The digital system has extreme flexibility from 10 to 90 channels may be programme for individual word rates of from 1.25 t $2 \pm 10°$ samples per second. System wor rates are 20, 10, 5, and 2.5 kc. The analog to-digital converter performs up to 2×10 conversions per second, depending on th selected sampling rate of the multiplexe Time-history and system-marker data ar also recorded. Provision for acceptance o Gray-code digital input data has been made The input on any channel may be low-leve (± 10 mv full-scale) or high-level (± 5 volt full-scale). Signal conditioning and auto matic calibration are provided. Multiplexe channel capacity can be extended by th addition of more modules. Pluggable pro gram boards provide flexibility of program

ng. The system is designed using all tran-orized components and is constructed to hstand vehicular environmental ex-mes. Detailed descriptions of the low-level e circuit, programming, accumulating, H coding techniques are given.

4
Sampled Data Processor, by A. R. Ras-assen (Scripps Inst. of Oceanography); *S. Govt. Res. Repts.*, vol. 33, p. 184(A), bruary 12, 1960; PB 143 613 (order from mi $3.00, ph $6.30).

A semi-automatic data sampler and com-ter accommodating two channels of in-rmation representing optically-stored, gnetically-stored, or direct electrical data the form of time-varying potentials is de-ibed. All data are converted to time-odulated pulses and directed to a com-ter where a combination of analog and ital computer circuits can be adjusted to rform a variety of mathematical opera-ns on the data with accuracies on the ler of ± 0.1 per cent. Results of the com-tations are displayed numerically on cimal totalizers, with the registered num-rs proportional to the computed functions.

5
Control System for Logical Block Diag-sis with Data Loading, by M. E. Senko BM Corp.); *Commun. Assoc. for Com-ting Mach.*, vol. 3, pp. 236–240; April, 60.

A section of an integrated diagnostic onitor system which facilitates the check-g of sections of instructions or subroutines ywhere in the object program is described. new method of specifying all diagnostic erations in a format similar to a computer ogram makes the system convenient to use d relatively simple to understand. A mber of other novel diagnostic features hich can be included in the system are also scribed.

6
n Automatic Analogue Computer for issile-Homing Investigations, by J. G. homason (ICI Central Instrument Lab.); *rans. Instrument Tech.*, vol. 12, pp. 16–21; arch, 1960.

An analog computer which operates and sets its parameters in response to an input ogram punched on paper tape, and which codes its results and punches them on an tput tape, is described. The output tape is ed as the input to a digital computer for ta processing (mainly statistical analysis) he computer was developed to eliminate e routine work necessary in computer in-stigation of guided missile system per-rmance and the tedious analysis of the mputer results.

7
se of a Digital Readout Unit in Converting pectrophotometric Data to Color Co-dinates, by F. W. Billmeyer, Jr. (E. I. Pont de Nemours and Co.); *J. Opt. Soc. m.*, vol. 50, pp. 137–143; February, 1960.

The use of a Librascope digital readout it for the General Electric recording spec-ophotmeter to enter spectrophotometric ta on IBM punched cards is discussed. he cards are used as input to an IBM 650 mputer to convert the color coordinates. The over-all precision of the spectrophotometer-digitizer-computer systems corresponds to 95 per cent confidence limits of about 0.001 in trichromatic coefficients x and y, or about 0.7 NBS units of color difference. Taking the results of the National Bureau of Standards as correct, the accuracy of the average of several measurements is within 0.0005 in trichromatic coefficients or 0.4 NBS units of color difference. The error frequency of the digitizer is currently below 1 in 7000 readouts and can be reduced to less than 1 in 200,000 readouts.

918
***XY* Plotting with the IBM Model 026 Printing Card Punch,** by R. Ehat and R. A. Taylor (Naval Radiological Defense Lab.) *U. S. Govt. Res. Repts.*, vol. 33, p. 184(A), February 12, 1960; PB 143 092 (order from LC mi $3.30, ph $7.80).

The adaptation of an IBM Model 026 Printing Card Punch to operate into a Mosely Model 30A Card Translator and a Mosely Model 2 Recorder is discussed. The design permits the plotting of IBM card information on an *XY* Plotter (Mosely Model 2) without disabling the normal card-punching and card-duplicating functions of the IBM Model 026 Printing Card Punch.

C-2: AUTOMATA—ARTIFICIAL

919
A Review of the Perceptron Program, by A. E. Murray (Cornell Aeronautical Lab., Inc.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 346–356; 1959.

A family of pattern recognition machines that can learn to discriminate several categories is described. The class name for these machines is "perceptron." After exposure to a few samples in a category, the machines tend to recognize spontaneously or classify correctly a new sample. Principal conclusions from past work are reviewed and plans for the future are indicated.

920
Synthesis of Minimal-State Machines, by S. Ginsburg (Hughes Res. Labs.); IRE Trans. on Electronic Computers, vol. EC-8, pp. 441–449; December, 1959.

A technique which yields a minimal-state machine satisfying a given set of behavioral specifications is presented. The machine is constructed in the same manner as has commonly been done in the past in synthesizing a "primitive flow table." This contribution consists not in describing a new method of synthesizing machines, but in showing that a particular instance of an established method yields a minimal-state machine. The basic synthesis technique may be slightly modified as so to be applicable to obtaining a minimal-state machine which has the stability conditions desired when working with unclocked circuits.

921
On the Synthesis of Finite Sequential Machines, by C. V. Srinivasan and R. Narasimhan (Tata Inst. of Fundamental Res., Bombay); *Proc. Indian Acad. Sci.*, vol. 50, sec. A, pp. 68–82; July, 1959.

Starting from the studies of Kleene and Mealy on sequential machines, a formalism which, in a sense, unifies their treatments is presented. From the specification of the required machine behavior in terms of events and associated output states, a uniform procedure is given for obtaining a transition table and from that a minimal machine, whenever such a complete reduction is possible. The various steps of the synthesis procedure are stated so that they can easily be programmed on a computer.

D-1: PROGRAMS—AUTOMATIC PROGRAMMING DIGITAL COMPUTERS

922
A New Approach to Small-Computer Programming and Control, by J. J. Lentz (IBM Corp.); *IBM J. Res. & Dev.*, vol. 2, pp. 72–83; January, 1958.

An approach to programming developed on the IBM 610 computer which enables a completely inexperienced operator to prepare complex problems by methods analogous to those used in desk calculators is described. The order structure is designed so that the operator can at all times communicate with the machine by short sentence-type instructions resembling the steps taken for solution by manual arithmetic. A special floating-decimal mode of operation permits the placing of the decimal point without elaborate programming.

923
Sequential Formula Translation, by K. Samelson and F. L. Bauer (Johannes Gutenberg Univ., Germany); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 76–83; February, 1960.

The syntax of an algorithmic language such as ALGOL is conveniently described as a sequence of states indicated by an element in the highest level of a special storage space called the symbols cellar. Transitions are controlled by admissible state-symbol pairs represented by a transition matrix. This view of syntax provides a simple rule for translating statements in the algorithmic language into the machine language. Sequential treatment of statements is not always possible in the case of certain optimizing processes such as recursive address calculation.

924
A Fortran-Compiled List-Processing Language, by H. Gelernter, J. R. Hansen, and C. L. Gerberich (IBM Corp.); *J. Assoc. for Computing Mach.*, vol. 7, pp. 87–101; April, 1960.

A compiled computer language, based on Fortran, for the manipulation of symbollic expressions is described. The algebraic structure of statements in the language corresponds closely to that of a Newell-Shaw-Simon list, making the generation and manipulation of complex expressions possible with a single statement. The language is applied to a geometry theorem-proving program, where its facility in handling intermediate data of unpredictable form, complexity, and length is particularly advantageous.

925
Symbolic Address-Symbolic Optimum Programs for a Drum-Memory Computer, by J. K. Russell (Naval Res. Lab.); *U. S. Govt. Res. Repts.*, vol. 33, p. 185(A), February 12, 1960; PB 151 999 (order from OTS $1.25).

A time-optimizing program for the Royal McBee LGP-30, a computer with magnetic-drum memory, is described. The optimizing process is performed on a data program written in a simple symbolic language (memory locations symbolized rather than specified). Although the data program is lengthened two to five times, it is one-fourth to one-third faster. Because of the length and lack of sequence in the resultant program, an additional program was developed to translate the symbolic language directly to unoptimized computer language (memory locations specified), for ease in trouble-shooting. Examples of the symbolic language are given, as well as the results of processing by the two programs.

926

A SAP-Like Assembly Program for the IBM 650, by A. E. Speckhard (IBM Corp.); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 2–5; January, 1960.

An IBM 650 assembly program similar in structure to that of the Share Assembly Program (SAP) used on the IBM 704 is described. Specific problems encountered are the handling of the instruction address of the 650 and relative addressing on a non-sequential machine. The former is solved by a special pseudo-instruction TRANSFER, and the latter by table look-up of the sequence of assigning memory cells to instructions.

D-2: PROGRAMS—APPLICATIONS, DIGITAL COMPUTERS

927

A New Method for the Payment of Bills and the Transfer of Credit, by G. Salton (Harvard Univ.); *J. Assoc. for Computing Mach.*, vol. 7, pp. 140–149; April, 1960.

A simplified method of processing utility company accounts is described. The present dual processing of payments both by the payee and by the banks involved in the transfer of credit is rejected in favor of a system in which the bill itself acts as the instrument of credit. The compatibility of the system with present banking practices, the anticipated advantages and disadvantages, the necessary authorizing guarantees, and the elimination of paper work are among the questions discussed.

928

Computer Rescues the Voting Process, by W. D. Bell (Tucson, Ariz.); *Control Engrg.*, vol. 7, pp. 65–69; February, 1960.

A solid-state ballot processor which can tabulate 600 ballots in 30 seconds is described. The machine was developed for use in Los Angeles County, Calif., to solve the ballot-counting problems peculiar to that county. In an election, the voter marks a specially prepared ballot in the conventional manner with a self-inking cross-shaped rubber stamp. During the tabulation, the ballots from each precinct are fed into the processor by a vacuum drum at a speed of 28,800 inches per minute. An ultraviolet source energizes the fluorescent ink; photoelectric cells read the ballot; and the processor corrects for skewness of the ballot by means of clock marks printed on each edge of the ballot, performs the logic necessary to validate a vote, counts, totals, and stores the vote for the precinct, and prints out the precinct total on IBM punched cards. The cards are then used to prepare final tabulations and official reports.

929

Use of the Stantec-Zebra Computer in Research, by R. A. J. Ord-Smith (Standard Telephones and Cables Co., Ltd.); *British Commun. and Electronics*, vol. 7, pp. 266–269; April, 1960.

Following a brief description of the Zebra computer and its Normal and Simple instruction codes, several research applications of the computer are discussed. These have included crystallographic calculations and the calculation of the probability of there being gold in a gold mine. A new and growing use is for research into computers themselves, both for developing new computers and for improving ways of programming existing computers. A table listing installations and applications of the Zebra computer is presented.

930

Solution of Systems of Simultaneous Linear Equations on the NAREC, by B. Lepson and J. P. Mason (Naval Res. Lab.); *U. S. Govt. Res. Repts.*, vol. 33, pp. 184–185(A), February 12, 1960; PB 140 974 (order from LC mi $2.40, ph $3.30).

Although several methods of solving large systems of simultaneous linear equations are known, the amount of computation required may be quite large. One of the standard methods, usually referred to as Gaussian elimination, has been adopted for high-speed computation and programmed for the NAREC. This can be used to solve, in a few minutes, systems of equations with as many as 54 unknowns. Several versions of this program are described in detail with instructions for their use.

931

The Properties and Methods for Computation of Exponentially-Mapped-Past Statistical Variables, by J. Otterman (Bell Telephone Labs., Inc.); IRE TRANS. ON AUTOMATIC CONTROL, vol. AC-5, pp. 11–17; January, 1960.

The value of exponentially-mapped-past (emp) statistical variables for statistical analysis of a process when the interest is focused on the recent behavior of the process is discussed. An exponential weighting function, decreasing into the past, is used in the case of continuously observed processes, and a geometric ratio is used in the case of discrete data. This approach is simplest from the point of view of ease of computation, and at the same time it has the advantage of some simple theoretical relationships, which are discussed. Analog computer circuits and digital computer flow diagrams which serve to compute the exponentially-mapped-past statistical variables are presented.

932

Tables of Values of the Modified Mathieu Functions, by E. T. Kirkpatrick (Univ. of Toledo); *Math. of Computation*, vol. 14, pp. 118–129; April, 1960.

The computation on an IBM 650 digital computer of the modified Mathieu functions which satisfy the modified Mathieu equation is discussed. The method of Ince and the Wolontis Interpretive System of coding were used. An IBM 650 program for computin the characteristic numbers, Fourier co efficients, and either the ordinary or modifie Mathieu function is available from th author on request and will be publishe separately. The computed values of th modified Mathieu function are listed.

933

Parabolic Approximation Method for Automatic Lens Design, by J. Meiron and G Volinez (Ministry of Defense, Israel); *J. Opt. Soc. Am.*, vol. 50, pp. 207–211; March 1960.

Lens design by the parabolic approxima tion method on the Weizmann Institute c Science digital computer (Weizac) is dis cussed. The method has definite advantage over the least-squares (see abstract 459) an steepest-descent methods, although the tim required for one iteration is double the cor responding time in the other methods. Ver little programming is required for the para bolic approximation method since most sub routines written for the least-squares metho can be utilized without any alteration.

934

A Program for Automatic Digital Computation of Transition Frequencies and Analysis of Microwave Rotational Spectra of Rigid Asymmetric Tops, by F. Kneubühl, T. Gäu mann, and H. H. Günthard (Swiss Federa Inst. Tech.); *J. Molecular Spectroscopy*, vol 3, pp. 349–362; August, 1959.

An automatic digital computer progran for the analysis of rotational transitions i described. Two problems are treated: 1) cal culations of desired transitions with given J K_{-1}, K_{+1} for arbitrary rotational constants and 2) evaluation of best-fitting rotationa constants from a number of measure transitions by the method of least squares The program reduces the time required fo numerical calculation of a rotational spec trum to a few hours. Comparison of result with existing tables and application to the microwave spectra of cyclopentanone an ethylene oxide illustrate the efficiency of the program.

935

Additional Nuclear Reactor Codes, by V. Nather and W. Sangren (Genera Atomics); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 6–19; January, 1960.

Abstracts of computer programs applica ble in the field of nuclear reactors are pro vided. The programs are coded according to company of origin and title, and are groupe under Burnup, Engineering, Group Diffu sion, Kinetics, Transport and Miscellaneous [See also Abstract 212.]

936

Simulation of Data-Switching Systems on a Digital Computer, by F. J. Gross (Bell Telephone Labs., Inc.); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78) pp. 796–800; January, 1960.

The use of digital computers to simulate the performance of data-message-switching systems is discussed. The operations for which the computer may be easily programmed are pointed out, and the programming of the computer to produce message characteristics suitable for use as inputs to the simulation is discussed. The simulation

a single-line teletypewriter selective call-
g system and of a multiline-data-switching
stem with one switching center is
scribed.

7
Digital Computer Program for Reducing ogical Statements to a Minimal Form, by . J. Butler, Jr. and J. N. Warfield (Univ. Kansas); *Proc. Natl. Electronics Conf.*, vol. , pp. 456–466; 1959.

A digital computer program that will duce logical statements of 19 or more vari-bles to a minimal expression is described. If unique minimal expression does not exist, e program is designed to present the alter-ative expressions so that the final choice of mplicity is left to the designer. The reduc-on method is a modification to the Harris ethod, which utilizes an *n*-dimensional ube for representing the logical statement. he computer program makes use of the irectional components present in the topo-gical representation of the logical state-ent. Simple relationships involving the irectional components that help to reduce he computer memory requirements and also o eliminate repetition of previously per-rmed operations are shown. Though ecifically intended for a computer, the ethod used in the program is quite con-enient without a computer. An illustrative xample is included.

38
se of High-Speed Digital Computers to tudy Performance of Complex Switching Networks Incorporating Time Delays, by . N. Chang and O. M. George (North merican Aviation, Inc.); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 8), pp. 982–987; January, 1960.

A control program for the simulation and nalysis of complex sequential switching net-orks on an IBM 704 computer and an ap-lication of the program to a simplified sys-em are described. The program utilizes Boolean algebra and takes into account the ctual time delays of the logical elements. Boolean algebra permits the state of each gic element to be determined at any time.

39
Recursive Functions of Symbolic Expres-ions and Their Computation by Machine, Pt. I, by J. McCarthy (Mass. Inst. Tech.); *Commun. Assoc. Computing Mach.*, vol. 3, p. 184–195; April, 1960.

A formalism for defining recursive func-ions is described, and a universal special unction which plays the theoretical role of Turing machine is defined. The computer epresentation of such functions by means of Newell-Shaw-Simon list structures is dis-ussed, and a general recursive function nterpretation of flow charts is given. The eneral features of an IBM 704 program, LISP, based on the above results are entioned.

40
The Automatic Creation of Literature Ab-tracts, by H. P. Luhn (IBM Corp.); *IBM . Res. & Dev.*, vol. 2, pp. 159–165; April, 958.

A method of extracting excerpts of tech-ical papers and magazine articles by auto-atic means to serve as abstracts is pre-sented. The complete text of the article is scanned by a data-processing machine and analyzed by means of a special program. Statistical information derived from word frequency and distribution is used to compute relative measures of significance, first for individual words and then for whole sentences. Sentences with the greatest relative significance are extracted to form an "auto-abstract" of the whole article.

941
Literary Data Processing, by P. Tasman (IBM Corp.); *IBM J. Res. & Dev.*, vol. 1, pp. 249–255; July, 1957.

A method for the rapid compilation of analytical indexes and concordances of printed works, using either a conventional punched card system or an electronic data processor, is presented. The procedures used in automatically analyzing and indexing the *Summa Theologica* of St. Thomas Aquinas are described in detail. Reference is also made to the indexing of the Dead Sea Scrolls, using the IBM 704 computer.

942
Computer Preparation of a Poetry Concordance, by J. A. Painter (Philco Corp.); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 91–95; February, 1960.

The computer preparation of a concordance of the poetry of Matthew Arnold is described. A poetry concordance is easier to mechanize than prose because a line of poetry provides a natural unit of context, thus avoiding the necessity for human pre-editing. After the elimination of common words such as articles, the remaining words of the text are arranged in alphabetic order, with the context and reference of each occurrence supplied. The printed output is photographed for reproduction by the photo-offset process.

943
A High-Speed Sorting Procedure, by R. M. Frank and R. B. Lazarus (Los Alamos Scientific Lab.); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 20–22; January, 1960.

A high-speed sorting procedure, initially due to D. L. Shell, for lists contained in internal memory is summarized. The method, which is based on a presort of the list into subsets and a subsequent interchanging of pairs, uses no additional memory space, and requires approximately $N \log_2 N$ rather than N^2 interchanges. A technique for further reducing the time of Shell's method is discussed.

944
Design of Logic for Recognition of Printed Characters by Simulation, by E. C. Greanias, C. J. Hoppel, M. Kloomok, and J. S. Osborne (IBM Corp.); *IBM J. Res. & Dev.*, vol. 1, pp. 8–18; January, 1957.

A logic for the recognition of printed characters by means of a proportional parts methods is presented. The identity of the character is determined by the relative size and position of character elements detected by optical scanning along closely packed vertical lines. The video information is coded to designate the number, size and position of the inked areas detected. The time sequence of this coded information is compared with prescribed sequences of given characters. A set of decoding definitions and the simulation of the process on an IBM 650 machine are discussed.

945
Digital Simulation in Perceptual Research, by E. E. David, Jr. (Bell Telephone Labs., Inc.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 322–328; 1959.

Several investigations using the technique of programming a digital computer to simulate a communications system with specified distortions to serve as material for subjective evaluation are reported. Using a data translator to provide an input-output link to the computer, the significant properties of several band-saving codings were obtained, with only modest programming and computing effort. A compiling routine to aid in programming similar problems has been devised; potentially this technique can be extended to generate complex stimuli for psychological exploration of perceptual mechanisms.

946
Perceptron Simulation Experiments, by F. Rosenblatt (Cornell Aeronautical Lab., Inc.); PROC. IRE, vol. 48, pp. 301–309; March, 1960.

An experimental program which uses the IBM 704 computer to simulate perceptual learning, recognition, and spontaneous classification of visual stimuli in the perceptron is described. The organization of simple perceptrons is briefly reviewed, and theoretically predicted performance curves are compared with those obtained from the simulation programs in several types of experiments designed to study "forced" and "spontaneous" learning of pattern discriminations.

947
A Program for Correcting Spelling Errors, by C. R. Blair (Dept. of Defense); *Information and Control*, vol. 3, pp. 60–67; March, 1960.

A program which uses a simple, heuristic procedure for associating "similar" spellings in order to correct misspelled words is discussed. Given only a vocabulary of properly spelled words, the computer can correct most (including unanticipated) misspellings without human assistance. Apart from practical applications, the process is interesting as an example of an unusual form of pattern recognition.

948
German Sentence Recognition, by G. H. Matthews and S. Rogovin (Mass. Inst. Tech.); *Mechanical Translation*, vol. 5, pp. 114–120; December, 1958.

A computer program which assigns one or more immediate analyses to a German sentence is described. An indication of which of all possible sentences any given sequence of words may represent is provided. All the information implicitly or explicitly contained in the sentence that can be used in the correct choice among its possible translations is extracted by the program.

949
Order of Subject and Object in Scientific Russian When Other Differentia Are Lacking, by D. G. Hays (The RAND Corp.);

Mechanical Translation, vol. 5, pp. 111–113, December, 1958.

The order of subject and object in the Russian sentence is shown to be an adequate criterion for distinguishing between them, when other grammatical properties lead to ambiguity. This conclusion is supported by a statistical analysis of apparently ambiguous cases.

950

Machine Translation in the Soviet Union by V. Yu. Rozentsveig (First Moscow State Pedagogical Institute of Foreign Language); *Mechanical Translation*, vol. 5, pp. 95–100; December, 1958.

Recent work in machine translation of languages in the Soviet Union is summarized. Dictionaries and translation algorithms for translation from English, Chinese and Japanese into Russian have been compiled, and a German-Russian algorithm is being developed. Efforts oriented toward the achievement of immediate, practical results, as well as theoretical problems of formal specification of linguistic structures are described.

951

A Survey of Soviet Work on Automatic Translation, by A. G. Oettinger (Harvard University); *Mechanical Translation*, vol. 5, pp. 101–110; December, 1958.

The Soviet literature on Automatic Translation is surveyed with the intention of acquainting English-speaking workers with sources of information about relevant Soviet work. Limited machine facilities restricted the range of practical accomplishment, but the standard of theoretical work is judged to be excellent. A comprehensive bibliography is provided.

D-3: PROGRAMS—TECHNIQUES, DIGITAL COMPUTERS

952

The Execute Operation—A Fourth Mode of Instruction Sequencing, by F. P. Brooks (IBM Corp.); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 168–170; March, 1960.

Four methods of sequencing computer instructions are summarized. In normal sequencing, each instruction has a unique successor defined either by an instruction counter or by a next instruction address. A second mode is the selection of an alternate sequence by branching, skipping or suppressing. Thirdly, sequencing is controlled by program interruption. Finally, a new mode of sequencing by means of Execute instructions which define a single, noninterrupting instruction which does not specify or imply its own successor, is described. Any instruction, including another Execute instruction, may be the object of an Execute instruction. In effect, a one-instruction subroutine is called and its return is specified. Specific applications are to subroutine and monitoring routines.

953

Optimum Coding 1103A Computer, by A. C. Hendrikson, J. G. Mackinney, and A. E. Roberts, Jr. (General Kinetics, Inc.); *U. S. Govt. Res. Repts.*, vol. 33, p. 294(A), March 18, 1960; PB 144 243 (order from LC mi $3.60, ph $9.30).

Detailed results of a study performed to develop an "optimum" coding for the ERA 1103A type high-speed electronic computer are presented. This coding is constructed to obtain characteristic values and vectors of symmetrical 2×2, 3×3, and 4×4 matrices (formed from coefficients of normal equations derived by least-squares methods). The coding is general and intended to separate two, three, or four nearly identical characteristic values. Provision is included for print-out of direction cosines, magnitude, square root of magnitude and its reciprocal; checks are made for orthogonality of vectors to six significant figures and agreement to ±10 units upon substitution in the original normal equations. Options for conversion of direction cosines to direction angles or to azimuth and elevation angles for print-out are supplied.

954

Systematic Scaling for Digital Differential Analyzers, by A. Gill (Univ. of California); IRE Trans. on Electronic Computers, vol. EC-8, pp. 486–489; December, 1959.

The usefulness of large-capacity digital differential analyzers (DDA's) is severely hampered because the scales needed for programming them must be compatible with the so-called "equilibrium," "topological," and "boundary" constraints imposed by the construction of the analyzer and the nature of the problem at hand. Simultaneous trial-and-error satisfaction of all these constraints, to achieve optimal range and accuracy of computation, is practically impossible for any problem involving more than a few integrators. A method of organizing the scaling constraints in a matrix form and of producing optimal scales in a systematic manner is described. The proposed scheme, which can be programmed for automatic execution, is adaptable for DDA's operating in conjunction with general-purpose digital computers.

D-4: PROGRAMS—TESTING, DIGITAL COMPUTERS

955

On Checking an Adder, by W. W. Peterson (Univ. of Florida); *IBM J. Res. & Dev.*, vol. 2, pp. 166–170; April, 1958.

Computer adders may be checked by a completely independent circuit, using check symbols that are residues of the numbers being added modulo a conveniently selected base. Such a residue error checking system is described. It is proved that all independent checking circuits for adders must be of the modular type. A method of handling residue-class checking symbols when overflow occurs is discussed.

D-5: PROGRAMS—APPLICATIONS, ANALOG COMPUTERS

956

Analogue Computer Techniques, by F. C. Harbert (Lewis Newark, Ltd.); *Electronic Engrg.*, vol. 32, pp. 74–77, February, 1960; pp. 166–169; March, 1960.

The analog computer arrangements required to solve simultaneous algebraic equations, eigenvalue problems, and polynominal equations using an interative method; a method for obtaining approximate solutions of partial differential equations by finite difference techniques; and the different computer arrangements required to simulate transportation delay using the Padé approximations are described. The latter is illustrated by an example showing the effect of such delay on the stability of a closed-loop system and a technique for counteracting its destabilizing effect.

957

Investigating Algebraic Equations Using Simulators, by V. M. El'iasberg; *Automation Express*, vol. 2, pp. 23–24; February, 1960.

An analog computer method for determining the graph of a specified polynomial is described. The method is based on reproducing the specified polynominal as the solution of the differential equation which defines it. The method makes it possible to achieve a direct determination of the real and imaginary roots of algebraic equations, to approximate the values of complex roots, and to study the stability characteristics of dynamic systems using the Mikhailov criterion.

958

An Electrical Analogue for the Torsion of Compound Bars, by S. C. Redshaw (Univ. of Birmingham, U. K.); *Proc. Second Internatl. Analogue Computation Meetings*, pp. 328–332; September 1–6, 1958.

The theory of the Saint-Venant torsion of certain composite bars is reviewed. Special attention is given to a case of interest to the aeronautical engineer, that in which a shell having a thin wall of one material is filled with, and bonded to, a core of dissimilar material. The use of a pure resistance network analog for the solution of this problem, which involves a boundary condition of the Fourier type, is described in detail. Experimental results are compared with a theoretical solution for the case of a bar having a rectangular cross section. Examples of torsional stiffness solutions for triangular and diamond-shaped sections, obtained by the use of the analog, are given and the results are compared with approximate theoretical solutions. An attempt at solving the problem by the use of conducting paper is also described.

959

The Computation of Correlation and Spectral Functions by Orthogonal Filtering, by E. G. Gilbert (Univ. of Michigan); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 954–959; January, 1960.

Lampard's series method for the computation of correlation and spectral functions is developed further. The series representation and its determination are reviewed. The relationship of time-domain and frequency-domain techniques to the series method; orthonormal approximating functions; analog computer circuits for orthonormal filtering; and approximation errors resulting from a finite number of terms in the approximating series, computer component errors, and finite averaging time are discussed.

960

Far Field Antenna Pattern Calculations by Means of a General Purpose Analog Com-

ıter, by A. I. Rubin and J. P. Landauer Electronic Associates, Inc.) and H. Q. otten (General Electric Co.); *Proc. Natl. lectronics Conf.*, vol. 15, pp. 995–1011; 959.

The complexity of antenna pattern calulations has in the past necessitated the se of the highest-speed and largest-capacity gital computers, such as the IBM 704. he core of the problem is the evaluation of surface integral of a complex vector inteand of the form $E(\theta,\phi)=\iint f(z,y,x)\exp\{-jg(z,y,\theta,\phi)\}dS$, where E is a complex ector, f is an ordinary vector dependent on ne horn pattern and the geometry of the ntenna surface, and g is a scalar measure of ne path length of a ray travelling from the orn to the reflector and thence to the aperure plane through the focus. The particular far-field point" is defined by coordinates θ, ; dS is the differential of the antenna surface. o determine the feasibility of carrying out hese calculations on an analog computer, he particular case of a circular paraboloid ntenna surface was chosen. Both "on-axis" nd "off-axis" horn locations were evaluated or far-field points in the principal θ, ϕ lanes. The analog computer program is hown in detail, and means of improving its fficiency are discussed. It is concluded that he analog computer can successfully comete with the IBM 704 in this general probem area, with the possibility of a cost reducion factor of from three to ten.

961
Analog Computer Design of Magnetic Amplifiers, by L. A. Gregory (Magnetic Controls Co.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 679–690; 1959.

Regardless of the mathematical approach used in the design of magnetic amplifiers, the multiple solution of several equations, some of which have nonlinear variables, is the cause of considerable time loss and error. Certain fundamental techniques in the analog solution of such equations which can minimize time and error are presented. The simultaneous solution of several equations involving common variables can be more quickly accomplished by substituting variable voltages as the counterpart of mathematical variables in these equations. The combination of these voltages according to mathematical rules can be read or recorded on any electrical measuring device and transformed back into original mathematical language to attain the desired design data.

962
Analog Computer Technique for Plotting Frequency Response, by J. L. Webster and D. L. Schultz (Chrysler Corp.); *ARS J.*, vol. 30, pp. 273–275; March, 1960.

A direct method of obtaining frequency response curves during analog computer studies is described. The system under study is driven by a constant-amplitude varying-frequency sine wave. System output is then rectified and recorded on the Y axis of a recorder whose X axis is swept at the same rate as that of the driving frequency. A suitable driving function can be generated using analog computer components.

E-2: MATHEMATICS—LOGIC—SYMBOLIC LOGIC, BOOLEAN ALGEBRA, NUMBER SYSTEMS

963
Floating-Point Arithmetics, by W. G. Wadey; *J. Assoc. Computing Mach.*, vol. 7, pp. 129–139; Aril, 1960.

Three types of floating-point arithmetics with error control are discussed and compared with conventional floating-point arithmetic. General multiplication and division shift criteria are derived (for any base) for Metropolis-type arithmetics. The limitations and most suitable range of application for each arithmetic are discussed.

964
A Normalized Floating Point Significance Checking Program, by G. P. Weeg and J. Eidson (Michigan State Univ.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 494–496; 1959.

In a normalized floating-point system, each number N is represented by $N=a\times r^b$ where $1/r\leq a<1$. After every arithmetic operation, the mantissa a is again returned to the range $(1/r, 1)$. In this process, digits may appear in the mantissa which seem to be significant but which may not be. To analyze the degree of significance of a floating-point mantissa, a program which determines an upper bound on error at each operation has been written. The procedures used in that routine are described and some facts discovered in its use are presented. The result of applying the routine to two matrix problems is given.

965
Arithmetic Operations for Digital Computers Using a Modified Reflected Binary Code, by H. M. Lucal (Univ. of Connecticut); IRE Trans. on Electronic Computers, vol. EC-8, pp. 449–458; December, 1959.

A method for performing the arithmetic operations of addition, subtraction, multiplication, and division using a reflected binary or Gray code, modified for integral numbers essentially by the addition of an even parity check bit, is presented. The modification facilitates both the arithmetic operations and the detection of errors—in the arithmetic process as well as in transmission. Although an adder using this code requires circuitry two or three times more complex than that of a conventional binary adder, it can be used also for subtraction with little additional circuitry and without complementation. In applications where reliability requirements justify the extra circuitry needed for arithmetic error detection, the modified reflected binary code may compare favorably with the conventional binary.

966
A Positive-Integer Arithmetic for Data Processing, by R. W. Murphy (IBM Corp.); *IBM J. Res. & Dev.*, vol. 1, pp. 158–170; April, 1957.

New arithmetic operations that yield non-negative results in computation are devised. An example is the diminish operation defined as $x\theta y=x-y$, *if* $x\geq y$ and $x\theta y=0$ if $x<y$. The applicability of these new operations to data processing is studied. The operations permit a wide variety of functions to be computed with fewer, and less complex, steps, and imply the feasiblity of constructing less complex, data-processing machines. In effect, tests on the signs of numbers are contained implicitly in the fundamental operations. The course of computation is thus fixed without the explicit use of branch instructions.

967
Proving Theorems by Pattern Recognition, I, by H. Wang (Bell Telephone Labs. Inc.); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 220–234; April, 1960.

A computer program to prove logical theorems by the method of pattern recognition is described. The program has yet to be extended to prove theorems of significant mathematical interest. In its present form it has proved 350 theorems from *Principia Mathematica* in less than nine minutes.

968
Matrix Algebra of Sequential Logic. Matrix Logic, III, by E. J. Schubert (Burroughs Corp.); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 1074–1079; January, 1960.

The use of matrix algebra in logical design is discussed. Matrix operations similar to function matrices for sequential circuits describing the behavior in the time domain are derived, and appropriate algebraic operations are introduced. The approach, believed to be novel, permits the computation of the output sequence for a given input sequence applied to a sequential circuit and its inversion, the computation of a function matrix required to produce a certain output sequence from a given input sequence.

969
Simultaneous Logical Equations. Matrix Logic, IV, by E. J. Schubert (Burroughs Corp.); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 1080–1083; January, 1960.

A new method for reducing logical problems of higher complexity based on matrix logic is presented. Sets of propositions related to a set of constraints are transformed into minimum form without iterative simplifications. The savings in design effort and hardware for the eventual circuit are demonstrated in an example.

970
Symmetric Switching Functions. Matrix Logic, V, by E. J. Schubert (Burroughs Corp.); *Commun. and Electronics*, No. 46 (*Trans. AIEE*, pt. I, vol. 78), pp. 1083–1087; January, 1960.

Symmetric logic functions are classified into ordinary and threshold functions. The first class is defined as being operative for only k of p inputs being active. Threshold functions are operative for at least k of p inputs. Ordinary symmetric and threshold functions are mutually related and one class may generate functions of the other class. Transistor circuits are already extensively used to perform threshold functions in form of resistor-coupled nonlinear amplifiers. Recently a new logical element which performs ordinary symmetric logic has been developed. To evaluate the merits of these logical elements efficiently, a method

which may be adapted to logical design by computer routines has been developed. Solution of problems involving up to ten variables is feasible without the aid of computers.

971
Detection of Group Invariance or Total Symmetry of a Boolean Function, by E. J. McCluskey, Jr. (Bell Telephone Labs.); *Bell Sys. Tech. J.*, vol. 35, pp. 1445–1453; November, 1956.

A method for determining the invariances, if any, of a Boolean function are presented; *i.e.*, whether any permutations and/or negations of the independent variables leave the function unchanged. The method is extended to the detection of totally symmetric functions.

972
Minimization of Boolean Functions, by E. J. McCluskey, Jr. (Bell Telephone Labs.); *Bell Sys. Tech. J.*, vol. 35, pp. 1417–1444; November, 1956.

A systematic procedure for expressing a Boolean function as a minimum sum of products is presented. The procedure is a simplification and extension of the method due to Quine. Only terms which differ in one variable are compared. Special attention is given to the so-called "don't-care" terms which can be included in the function solely for the designer's convenience.

973
A New Concept in Computing, by R. Lindaman (Remington Rand); PROC. IRE, vol. 48, p. 257; February, 1960.

The design of majority-element logic networks by the conversion of conventional Boolean expressions to equivalent expressions in "majority form" is discussed. An expression is in majority form if it is expressed exclusively in terms of Boolean literals (with and without negation), grouping symbols such as parentheses, and the majority decision operator. A conversion method for networks having no more than three inputs, no more than three inputs per element, and no storage function is described and illustrated by the derivation of majority-element networks for a parity checker and a binary adder stage. The networks are somewhat simpler than those developed by Wigington's method (see abstract 370).

974
A Mechanical Proof Procedure and its Realization in an Electronic Computer, by D. Prawitz, H. Prawitz, and N. Voghera; *J. Assoc. for Computing Mach.*, vol. 7, pp. 102–128; April, 1960.

A method for mechanizing the proof procedures of the predicate calculus is described. The predicate calculus, unlike the propositional calculus (also known as the sentential calculus or Boolean algebra) which is the only logic so far applied in computers, is sufficient for the expression of most mathematical deductions. The logical theory behind the proof method is given in the form of a pseudo-program. The problem of realizing this pseudo-program in a computer is discussed, and various applications, together with theorems proved by the method, are presented.

975
Multivalued Switching Algebras and their Application in Digital Systems, by E. I. Muehldorf (Westinghouse Electric Corp.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 467–480; 1959.

A brief survey of ternary switching algebras is presented. These algebras can be based on Post's modular algebra, but for practical reasons it is useful to change the concept and base the algebra on the so-called $j_k(x)$ functions as defined by Rosser and Turquette. A practical ternary switching algebra is extended to m values with emphasis on multivalued devices. A set of logic circuits capable of performing nonbinary logical operations is given. Application of nonbinary switching circuitry to digital systems such as computers and communication systems is shown, and the differences between the two applications are pointed out.

976
A Note on the Number of Internal Variable Assignments for Sequential Switching Circuits, by E. J. McCluskey, Jr. and S. H. Unger (Bell Telephone Labs., Inc.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 439–440; December, 1959.

An important step in the synthesis of sequential switching circuits is the assignment of binary variable states to represent internal states of the circuit. A formula which indicates the number of different assignments possible for flow tables having a given number of rows is derived. There are only three essentially different assignments possible for a four-row table, and there are 140 for a five-row table.

977
Synthesis of Series-Parallel Network Switching Functions, by W. Semon (Harvard Univ.); *Bell Sys. Tech. J.*, vol. 37, pp. 877–898; July, 1958.

A network function is defined as a switching function of n variables, with no variables vacuous, which can be realized by a network containing n switches. From the switching functions of n variables the network functions are abstracted, and the properties of those network functions corresponding to series-parallel networks are studied. A convenient method for synthesis is developed.

978
The Application of Digital Computer Techniques to Electronic Automatic Telephone Switching Systems, by D. K. Melvin (General Telephone Labs., Inc.); *Proc. Natl. Electronics Conf.*, vol. 15, pp. 593–605; 1959.

The basic principles of crosspoint and time-division-multiplex electronic telephone switching systems are described with emphasis on the digital computer techniques used in controlling the voice transmission paths. The requirements for logic, temporary and permanent memory, recirculating memories, register, and buffer storage are discussed. Time sharing of control equipment, which enables dial pulses from many subscribers' telephones to be registered simultaneously, is also possible with these high-speed techniques. A recirculating magneto-striction delay line which records dial pulses and remembers the appropriate time-slot to be used for multiplex transmission is compared with a recirculating ferrite core memory which serves a similar purpose. The advantages of using Boolean algebra in the design of electronic telephone systems for reducing the number of components and simplifying the resulting circuitry are discussed.

979
A Note on the Use of the Abacus in Number Conversion, by H. Kanner (Univ. of Chicago); *Commun. Assoc. for Computing Mach.*, vol. 3, p. 167; March, 1960.

The conversion of integers in both directions from the base ten to any desired base by means of the abacus is described and illustrated by examples. The procedures are far less cumbersome than the corresponding operations on an electric desk calculator.

E-3: MATHEMATICS—LOGIC—NUMERICAL ANALYSIS

980
On the Utility of Newton's Method for Computing Complex Roots of Equations, by I. M. Longman (Weizmann Inst. Sci.); *Math. of Computation*, vol. 14, pp. 187–189; April, 1960.

It is pointed out that equations with complex roots can be easily solved on high-speed computers by Newton's method of numerical solution of equations. Two examples solved on the Weizac computers are given.

981
Methods for Fitting Rational Approximations, Part I: Telescoping Procedures for Continued Fractions, by H. J. Maehly (Princeton Univ.); *J. Assoc. for Computing Mach.*, vol. 7, pp. 150–162; April, 1960.

Three closely related methods for adjusting the coefficients of a truncated continuous fraction so that the maximum value of the absolute error, on a given interval, is nearly minimized are presented. The methods correspond to the well-known series economization techniques of Lanczos in the case of power series. The computations for the corrections of the coefficients are simple, but a "true" Tchebycheff approximation is attained only if the interval of approximation is very small.

982
A Necessary and Sufficient Condition for Stability of Partial Difference Equation Problems, by R. E. Esch (Harvard Univ.); *J. Assoc. for Computing Mach.*, vol. 7, pp. 163–175; April, 1960.

Richtmyer's conditions for the stability of numerical methods for solving partial differential equation problems are reviewed. These conditions include the so-called Von Neumann necessary condition and several alternative sufficient conditions. By use of the Jordan canonical decomposition, a simpler condition which is both necessary and sufficient, and which includes Richtmyer's conditions as special cases, is developed.

983
A Modification of Filon's Method of Numerical Integration, by E. A. Flinn (Aus-

ilian Natl. Univ.); *J. Assoc. for Comput-g Mach.*, vol. 7, pp. 181–184; April, 1960.

Filon's method of numerical integration r integrals of the form $I=\int_A^B f(x)\cos px dx$, p rge, uses a modified Simpson's rule on an nterval no longer than is required to inte-ate $\int_A^B f(x)dx$ alone to the desired accuracy. he modification described was developed evaluate integrals of the form $F(T)=\int_0^T f(x)\cos dx$ using a larger interval an is possible with Filon's formula. A th-order instead of a second-order curve fitted to the middle and end points of each ndividual panel.

984

omputation of e^N for $-\infty<N<+\infty$ sing an Electronic Computer, by E. G. Kogbetliantz (IBM Corp.); *IBM J. Res. Dev.*, vol. 1, pp. 110–115; April, 1957.

Both rational and polynomial approxi-nations that allow the exponential function e^N to be computed for any value of the xponent N from minus infinity to plus in-nity in a minimum number of operations re studied. This minimum is attained ithout unduly increasing the number of recomputed constants to be stored and lso without limiting the number of first orrect significant digits. Formulas appli-able to both decimal and binary machines re considered.

985

Numerical Inversion of Laplace Transforms, by L. A. Schmittroth (Phillips Petroleum Co.); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 171–173; March, 1960.

A method for computing the inverse of a Laplace transform $F(S)$ when it is known that all the singularities of $F(S)$ lie in the left half-plane is described. The method is useful when the classical poles and residues method of complex integral evaluation is computationally prohibitive. A procedure of resolution into trigonometric integrals in preparation for numerical integration by Gaussian quadrature is presented. The method may be modified for positive poles and small negative poles.

986

A Starting Method for the Three-Point Adams Predictor-Corrector Method, by R. Alonso (Mass. Inst. Tech.); *J. Assoc. for Computing Mach.*, vol. 7, pp. 176–180; April, 1960.

In methods such as Adams' three-point predictor-corrector method for solving ordinary differential equations, considerable programming work is required in separate procedures for determining starting values. A method whereby the three-point Adams formula may be considered self-starting is presented. Minor modifications provide starting values of sufficient accuracy for continuing the solution.

E-5: MATHEMATICS—LOGIC—INFORMATION THEORY

987

Information-Theoretical Aspects of Inductive and Deductive Inference, by S. Watanabe (IBM Corp.); *IBM J. Res. & Dev.*, vol. 4, pp. 208–231; April, 1960.

By a straightforward application of Bayes's theorem of probability, the behavior of credibilities (inductive probabilities) of competing hypotheses as functions of an increasing body of relevant empirical data is discussed. The effect of *a priori* credibilities is shown to persist in the evaluation of credibilities in general, except in the important limiting cases investigated. An "inverse H-theorem" is mathematically demonstrated, according to which the entropy function defined in terms of the credibilities shows a net decrease in time. This decrease is not necessarily monotonous in an individual case, but is monotonous in the "expected" behavior of the inductive entropy function. Three machine-simulation experiments of inductive inference on the IBM 704 are described. The first two concern the classical problem of guessing the ratio of white and black balls in an urn. The third experiment concerns guessing a hidden pattern obeyed by a sequence of binary numbers.

988

Computer Music, by L. A. Hiller, Jr. (Univ. of Illinois); *Scientific American*, vol. 201, pp. 109–114, 116–120; December, 1959.

The role of information theory in the composition of music on a computer is discussed, and a series of experiments in composition carried out on the ILLIAC high-speed digital computer at the University of Illinois are described. In these experiments, random integers were generated and screened for redundancy by means of programs which embodied arithmetical analogs of rules of composition. The integers which passed the screening were stored in the computer memory until the composition of the melody was completed. If the computer could not complete the melody without breaking the rules, its memory was cleared and the composition started again. It is suggested that with a more elaborate program a symphony can be composed.

989

An Example and Extension of Capacity Calculation of a Certain Discrete Channel with Memory, by S.-H. Chang and P. G. McHugh (Northeastern Univ.); *U. S. Govt. Res. Repts.*, vol. 33, p. 294(A), March 18, 1960; PB 144 419 (order from LC mi $2.70, ph $4.80).

Previous work on the capacity of a certain binary channel with finite memory is extended. To illustrate the method of capacity calculation, a channel is devised with two types of imperfections: distortion resulting from memory, and contamination caused by noise. The relative effects of noise and memory are demonstrated, as well as the increase of capacity by tolerating a greater interdigital interference and the use of pulse weighing to counteract the effect of memory. The method of calculation is further extended from the binary channel to the m-nary channel.

990

The Use of Coset Equivalence in the Analysis and Decoding of Group Codes, by E. Prange (A. F. Cambridge Res. Center); *U. S. Govt. Res. Repts.*, vol. 33, p. 293(A), March 18, 1960; PB 143 967 (order from LC mi $3.00, ph $6.30).

For an error-correcting code Group A, the Group G of coordinate permutations that map A onto itself is used to define an equivalence relation on A-cosets. It is shown that this equivalence relation can be used in the analysis of the error-correcting properties of A, and in the definition and verification of operationally feasible decoding algorithms that satisfy the minimal distance criterion. Decoding algorithms under a (weak) block-length criterion are also considered for a special class of group codes. Applications are made to some specific codes, the largest being a code in two symbols whose words have 45 information and 28 check positions.

991

Gray Codes and Paths on the n-Cube, by E. N. Gilbert (Bell Telephone Labs.); *Bell Sys. Tech. J.*, vol. 37, pp. 815–826; May, 1958.

A generalized Gray code may be considered as one in which successive code points are distinct binary n-tuples such that each differs from its predecessor in just one coordinate. Geometrically, such a set of code points corresponds to a path which follows edges of an n-dimensional cube. A process for finding all types of closed paths on cubes with $n\leqq 4$ is presented. For larger n, the process given will produce large numbers of paths.

992

A Class of Binary Signalling Alphabets, by D. Slepian (Bell Telephone Labs.); *Bell Sys. Tech. J.*, vol. 35, pp. 203–234; January, 1956.

A class of binary signalling alphabets (or codes) called group alphabets is described. The alphabets, which are generalizations of Hamming's error- correcting and -detecting codes, possess the following special features: 1) the encoding is simple to realize; 2) all letters are treated alike in transmission; 3) maximum likelihood detection is convenient to instrument; and 4) for certain practical cases no better alphabets exist. The group alphabets of length $\leqq 10$ binary digits are compiled.

993

On a Class of Error Correcting Binary Group Codes, by R. C. Bose and D. K. Ray-Chaudhuri (Univ. of North Carolina and Case Inst. Tech.); *Information and Control*, vol. 3, pp. 68–79; March, 1960.

A general method of constructing error-correcting binary group codes is obtained. A binary group code with n places, k of which are information places, is called an (n,k) code. An explicit method of constructing t-error-correcting (n,k) codes is given for $n=2^m-1$ and $k=2^m-1-R(m,t)\geqq 2^m-1-mt$, where $R(m,t)$ is a function of m and t which cannot exceed mt. An example is worked out to illustrate the method of construction.

994

Non-Binary Error Correction Codes, by W. Ulrich (Bell Telephone Labs., Inc.); *Bell Sys. Tech. J.*, vol. 36, pp. 1341–1388; November, 1957.

Codes for correcting single small errors, and for correcting single small errors and detecting double small errors, in a message of arbitrary length, for an arbitrary number of different signals in the channel are derived. Codes for detecting single unrestricted errors are also discussed. Finally, a set of codes based on the Reed-Muller codes for

correcting a number of errors in a restricted class of message lengths is described. All the codes considered are readily implemented.

J: SUMMARIES AND REVIEWS

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Russian Visit to U. S. Computers, by E. M. Zaitzeff (Bendix Systems Div.) and M. M. Astrahan (IBM Corp.); IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-8, pp. 489–497; December, 1959.

In April and May of 1959, an exchange of visits by computer experts took place between the U. S. and the U.S.S.R. The series of negotiations which led up to this exchange is described, as is the visit of the Russian delegation to America. [For a report of the visit of the U. S. delegation to Russia see the following abstract.]

996

Soviet Computer Technology—1959, W. H. Ware, Ed.; *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 131–166, March, 1960; IRE TRANS. ON ELECTRONIC COMPUTERS, vol. EC-9, pp. 72–120; March, 1960.

A detailed account of a visit of a U. S. technical delegation to study computers in the U.S.S.R. is presented. The itinerary, descriptions of specific Soviet computers and computing centers, a discussion of Russian computer education, and details of current circuit and component development are included. The instruction set of the URAL-I and URAL-II machines, an analysis of magnetic core work, and a bibliography of relevant Soviet documents are provided.

997

Mathematical Investigations Related to the Use of Electronic Computing Machines, by A. A. Liapuno; (Moscow Univ.) (translated by M. D. Friedman); *Commun. Assoc. for Computing Mach.*, vol. 3, pp. 107–118; February, 1960.

A review of the main areas of endeavor in the computing sciences in the Soviet Union is presented. The subjects discussed include theoretical investigations in programming, nonarithmetic uses of computers, control systems, and cybernetics.

AUTHOR INDEX

SUBJECT INDEX

PGEC News

To All PGEC Chapter Officers

The PGEC *News* page of these TRANSACTIONS is open for your announcements and report of activities. Deadline is the first of the month, two months ahead of the date of issue. Send all items to the *Editor*.

PGEC COMMITTEE APPOINTMENTS

New committee appointments announced by PGEC Chairman Arnold Cohen at the August 24 Administrative Committee meeting at WESCON are as follows: 1) Walter L. Anderson, Conferences and Symposia Committee Chairman (a reactivation of the old meetings committee), 2) Werner Buchholz, Publications Advisory Committee Chairman, 3) Frank Heart, Awards Committee Chairman, 4) Willis H. Ware, Chairman of a new Intersociety Relations Committee, and 5) E. C. Johnson, PGEC Representative on the Technical Program Committee for the 1961 IRE International Convention.

AFIPS

The proposed new constitution for the American Federation of Information Processing Societies was discussed at the August 24 PGEC Administrative Committee meeting at WESCON. Action was deferred pending clarification of several points of substance by the PGEC representatives to NJCC. A mail ballot on the constitution is planned at an early date in order to bring appropriate recommendations before the IRE Executive Committee.

NEXT ADMINISTRATIVE COMMITTEE MEETING

The next meeting of the PGEC Administrative Committee, will be held on the eve of the Eastern Joint Computer Conference, and is scheduled for 7:30 P.M., December 12, 1960, at the Hotel New Yorker, New York, N. Y.

CHAPTER MEETING SUPPORT

PGEC Chapter Chairmen might like to be reminded that an extra $10.00 per chapter meeting is available to help defray costs. This amount supplements the normal $10.00 available from IRE for any PG chapter meeting, and is paid under the same rules and regulations, through the local IRE Section.

PGEC BIBLIOGRAPHY PROJECT

PGEC chapters are invited to undertake special-purpose bibliographies on advanced topics in the computer field, for publication in IRE TRANSACTIONS ON ELECTRONIC COMPUTERS.

For further information, contact

Dr. L. F. Jones
Norden Div.
United Aircraft Corp.
Milford, Conn.

BOSTON CHAPTER NEWS

A meeting of the Boston Chapter of PGEC was held on June 29, 1960, at which new officers were elected. Members of the executive committee are John T. Gilmore, Jr., William A. Hosier, Hawley K. Rising, Alfred K. Susskind, and Alexander Vanderburgh. Chapter officers elected were Peter Calingaert, chairman; Alfred Susskind, vice-chairman; Alex Vanderburgh, secretary; and Richard K. Bennett, treasurer. The following committee chairmen were appointed: Richard K. Bennett, planning; John T. Gilmore, publicity; and Hawley K. Rising, membership.

REPORT OF BOSTON PGEC MEMBERSHIP SURVEY

On August 7 1959, the Boston Chapter of PGEC mailed to each of its 594 registered members a one-sheet (two sides) questionnaire with stamped return envelope, in an attempt to find out where the interests of most of its members lay, to solicit suggestions for chapter activities, and to learn the names of those members willing to take an active part in carrying on those activities. By this means the officers of the chapter hope to promote member interest and to schedule activities better tailored to satisfy and maintain such interest.

205 of the questionnaires were returned; we are summarizing the replies here in the thought that the questions and the nature of the answers will interest not only PGEC members but also other professional groups confronting similar problems of planning.

Question 1, General Field of Interest, elicited a 185 to 21 preference of digital to analog topics, plus 16 assorted other votes for such fields as hybrid computers and A-D converters. Although we had expected a digital preference, we had not expected it to be so marked.

The second question concerned attendance. 83 of the respondents had attended no meetings last year, with the remainder averaging about $2\frac{2}{3}$ meetings, of which 20 had attended four or more. Nearly all expected to attend some of the current year's meetings, about three meetings out of a presumed six on the average. Roughly half of the respondents indicated probable attendance at the first two meetings. It thus appears that average attendance at last year's meetings was about 45. Judging by the number of returned questionnaires, somewhat over 200 of our 594 registered members have a close interest in Boston Chapter activities; lack of interest by the balance is in part because many of them live too far away. Of these, from 100 to 150 seem to be attenders of meetings, and for any given meeting, perhaps $\frac{1}{2}$ to $\frac{1}{3}$ of those intending to come do actually remember and find themselves able to appear.

In the absence of indications to the contrary, we conclude that the traditional six meetings per season are a satisfactory number.

On question 3, time and place of meetings, preference ran to Cambridge, Boston, and the western segment of Route 128. We had hoped to obtain a few bright new suggestions for meeting places; we got none. Replies leaned strongly to MIT and Harvard, MIT leading by 2 to 1. Doubtless this is because most members are engineers, many being MIT graduates. Rooms at Harvard and MIT cost about the same; with the possible exception of the new Vannevar Bush room at MIT, accomodations are better at Harvard, and for the present we will plan to hold meetings there.

Only 18 of the 205 replies regarded cocktail and dinner facilities as a desirable adjunct to the meeting locale. Mean time preference for starting meetings was very close to 7:30, with few voting for before 7 or after 8.

The fourth question set forth ten areas of interest, and it is probably worth listing them in order of preference with the number of first choices accorded each. (Rank was assigned by weighting 1st, 2nd, and 3rd choices)

Topic	No. First Choices
Entire Computing Systems	46
Circuits	44
Logical Design	44
Real-Time Control Applications	37
Components	36
Scientific and Engineering Applications	17
Input-Output Devices	20
Programming Methods	13
Business and Kindred Manipulative Data-Processing	19
Numerical Methods	6

These preferences show the strong engineering background of the people replying. One inference we draw is that the PGEC is not reaching the large number of people in this area who are oriented towards programming and computer applications. The possibility of enlarging PGEC scope to attract these people, a large number of whom are not engineers and hence not IRE members, seems worth exploring.

In answer to the fifth question, whether members preferred to hear broad survey talks or detailed discussions of specific equipment, opinion was equally divided (91 to 108). One significant observation here was that the caliber of the speaker was more important than the degree of specialization of his topic.

In the sixth question, members were asked to state whether they would like to see joint meetings held with other professional groups, and if so, to indicate which groups. Of 171 replies to this question, only 17 said no; the rest were split, 77 to 77, between favor and indifference. The number of votes accorded to the five groups listed were as follows:

Automatic Control	92
Information Theory	73
Communications Theory	49
Electron Devices	43
Microwave Theory	14

20 other miscellaneous votes were cast, suggesting such other groups as engineering management, instrumentation, and medical electronics.

The preference for Automatic Control was not surprising, but it is perhaps strange that Electron Devices did not come out higher. This question plus the previous one on meeting topics point strongly to at least one meeting on real-time control, hopefully a joint one.

On the seventh question, an invitation to suggest ways in which members would like to see chapter activities expand, about two-thirds of respondents left the space blank; those replying leaned strongly to trips and workshops, with a few other suggestions such as lecture series. In general these replies were not particularly useful, nor did they contain any new ideas.

The final item, an invitation to volunteer active participation in PGEC activities, elicited 48 volunteers and 117 definite non-volunteers, and the rest left the item blank. This large number of volunteers was perhaps the most beneficial single result of the survey; building on it, we have started a number of new committees and hopefully will start a few new activities.

Were we to repeat the questionnaire, we might improve it by at least adding a question on present occupation and print "over" at the bottom of the first side. It might also have been useful to ask about membership in other professional societies.

In general, response to the questionnaire and the level of interest indicated surpassed our expectations; we felt that it was well worth the small effort and $50 or so of mailing expense that it cost.

AUERBACH HEADS IFIPS

Isaac L. Auerbach, long active in PGEC and IRE affairs, has been elected first President of the International Federation of Information Processing Societies at its recent meeting in Rome, Italy. Mr. Auerbach is the United States representative to IFIPS, acting for NJCC and its sponsoring societies, IRE, AIEE, and ACM. (In the ordinary work-week, Ike Auerbach is President of Auerbach Electronics of Philadelphia and New York City.)

Eleven member nations of IFIPS each sent a delegate to the Rome meeting to plan the next International Conference on Information Processing, to be held in Germany in 1962.

Notices

This *Notices* Section is open to all who have an announcement of a conference, symposium, session, publication, or other artifact of interest to the PGEC membership. Please send announcements to the *Editor*, who will put them in the first available issue. The right is reserved to edit the announcements, and to decide whether they indeed are aimed at our audience.

OMING MEETINGS

IEE SYMPOSIUM ON SWITCHING IRCUIT THEORY AND LOGICAL ESIGN

The symposium will consist of sessions ld during the AIEE Fall General Meeting Chicago, October 9–14, 1960. For further formation, write to Thomas H. Mott, Jr., CA Laboratories, Princeton, N. J.

960 NONLINEAR MAGNETICS AND AGNETIC AMPLIFIERS ONFERENCE

The Technical Program for the 1960 onlinear Magnetics and Magnetic Amplirs Conference has been announced. Three ssions are of particular interest to people the computer field. For further informapn, write Carl W. Green, Publicity Chairlan, Bell Telephone Laboratories, Inc., loom 3C-130, Whippany, N. J. A partial sting of the program follows:

Wednesday, October 26, 1960
ession I. 10:00 a.m.
omputer Magnetics—Part 1
hairman: R. O. Endres, Reese Engineering Co., Philadelphia, Pa.

) "Distributed Parameter Aspects of Core Memory Wiring," J. S. Eggenberger, IBM, Poughkeepsie, N. Y.
) "Domain Behavior in Thin Magnetic Films," J. W. Hart, Burroughs Corp., Paoli, Pa.
) "Optical Readout of Digital Magneitc Recording," J. J. Miyata, National Cash Register Co., Hawthorne, Calif.
) "Magnetics in Doppler Signal Data Extraction," R. J. Metz, J. G. Fay, Air Arm Div., Westinghouse Electric Corp., Baltimore, Md.

ession II. 2:00 p.m.
omputer Magnetics—Part 2
hairman: R. R. Booth, IBM, Ossining, N. Y.

) "A New Magnetic High-Speed Switching Element—Its Application to Machine Tool Numerical Positioning Control," M. Dumaire, Societe D'Electronique Et D'A Ultomatisme, Seine, France.
2) "Poly-Aperature Cores Used in Non-Destructive Read-Out Counter," W. R. Johnston, Telemeter Magnetics, Culver City, Calif.
3) "Self-Propagating Core Logic," A. S. Myers, Jr., Product Development Lab., IBM, Poughkeepsie, N. Y.
4) "MAD-Resistance Type Magnetic Shift Registers," D. R. Bennion, Stanford Research Inst., Menlo Park, Calif.
5) "Analysis of MAD-R Shift Register and Driver," D. Nitzan, Stanford Research Inst., Menlo Park, Calif.

Thursday October 27, 1960
Session III. 9:00 a.m.
Nonlinear Magnetics
Chairman: G. C. Feth, General Electric Corp., Schenectady, N. Y.

1) "A Magnetic Device for High-Speed Sensing of Small Currents," J. A. Baldwin, Jr., Bell Telephone Laboratories, Inc., Murray Hill, N. J.
2) "Behavior of Magnetic Materials Under Extreme Environmental Conditions," AIEE Report.
3) "An Improved Model for Flux Reversal in Ni-Fe Cores," I. Leliakov, General Electric Co., Syracuse, N. Y., F. J. Friedlaender, Purdue University, Lafayette, Ind.
4) "A Saturable-Core Modulation Integrator," R. C. Barker, A. J. Gruodis, Yale University, New Haven, Conn.
5) "High Repetition Rate Magnetic Pulse Generators," B. M. Wolffram, Magnetic Research Corp., Hawthorne, Calif.
6) "Relaxation Oscillations at Multiple Frequencies of Even Subharmonics," N. S. Prywes, University of Pennsylvania Moore School of Engrg., Philadelphia, Pa.

Session IV. 2:00 p.m.
Magnetic Amplifiers
Friday, October 28, 1960
Session V, 9:00 a.m.
Combined Semiconductors and Nonlinear Magnetics

POWER INDUSTRY COMPUTER APPLICATIONS CONFERENCE

The Second Power Industry Computer Applications Conference sponsored by AIEE will be held in St. Louis, November 9–11, 1960. Complete details are available from E. L. Harder, Analytical Department 4113, Westinghouse Electric Corp., East Pittsburgh, Pa.

1960 EASTERN JOINT COMPUTER CONFERENCE

The 1960 Eastern Joint Computer Conference will be held December 13–15 at the Hotel New Yorker and the Manhattan Center in New York, N. Y. This tenth Eastern Joint meeting will stress papers describing significant and interesting accomplishments in the field. No parallel sessions are planned. A $300 prize will be awarded for the best presentation of a paper at the Conference. For additional information, write to

Jack Haney
General Telephone and Electric Co.
730 Third Avenue
New York, N. Y.

1961 IRE INTERNATIONAL CONVENTION

New York Coliseum and Waldorf-Astoria Hotel, March 20–23, 1961.

SYMPOSIUM ON COMBINED ANALOG AND DIGITAL SYSTEMS

A Symposium on combined analog and digital computing systems will be held in Philadelphia on December 16–17, 1960, right after EJCC. The meeting is sponsored jointly by Simulation Councils, Inc., and the General Electric Co. For further information contact,

Mr. Marty Paskman
General Electric Co.
Missiles and Space Div.
Philadelphia 4, Pa.

WESTERN JOINT COMPUTER 1961 CONFERENCE SLATED

The annual Western Joint Computer Conference has been scheduled for May 9–11, 1961, at the Ambassador Hotel, Los Angeles, Calif., Dr. Walter F. Bauer, is General Chairman.

The theme of the conference and exhibits, "Extending Man's Intellect," is planned to bring out new techniques and applications for automatic information processing equipment.

"The use of computers and data processing equipment," Bauer said, "is being directed to the replacement of human activities in complex scientific and business operations and will eventually have a profound effect on the national economy." The 1961 meeting of the WJCC will emphasize equipment design, uses, and functions in new areas of computer applications.

The annual conference is sponsored by the National Joint Computer Committee formed by representatives of the IRE, the AIEE, and the Association for Computing Machinery. The committee sponsors an Eastern and a Western meeting each year.

Bauer also named his Vice Chairman, Keith Uncapher, of the RAND Corporation, Santa Monica, Calif. Dr. Robert W. Rector, Space Technology Laboratories,

will join Bauer and Uncapher on the executive committee as conference administrator.

Prof. Cornelius Leondes, Department of Engineering, University of California at Los Angeles, is in charge of the conference program. He is being assisted by Smil Ruhman, chief electronic engineer, Packard Bell Computer; John D. Madden, director of information processing, System Development Corp., and Paul Armer, head of the computer sciences department, The RAND Corp.

Chairmen of arrangements committees for the conference include: publication, R. D. Aeder, IBM Corporation, Los Angeles; hotel arrangements, William Dobrusky, System Development Corporation; finance, William S. Speer, Electronic Engineering Data Systems, Norden Division, United Aircraft Corporation, Gardena; public relations, Santo Lanzarotta, Datamation Magazine; registration, Marvin Howard, Ramo-Wooldridge, Canoga Park; exhibits, R. H. Hill, Ramo-Wooldridge, Canoga Park; printing, L. C. Hobbs, Aeronutronic Division, Ford Motor Company, Newport Beach; trips, Joel Herbst, Telemeter Magnetics, Culver City; and women's activities, Mrs. Phyllis Huggins, Bendix Computer Division, Bendix Corporation.

The WJCC is the largest conference on the West Coast devoted to information processing techniques and equipment. The 1960 meeting in San Francisco drew over 2000 registrants and an additional 700 exhibitor personnel.

For further information write:

Dr. Walter F. Bauer, General Chairman
Ramo Wooldridge
8433 Fallbrook Avenue
Canoga Park, Calif.

CALLS FOR PAPERS

1961 IRE-AIEE-U OF P INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

The 1961 International Solid-State Circuits Conference, the 8th annual such meeting will be held February 15–17, 1961, on the campus of the University of Pennsylvania and at the Sheraton Hotel, Philadelphia, Pa.

The conference, sponsored jointly by the IRE, AIEE, and University of Pennsylvania, will feature papers dealing with circuit properties, circuit philosophy and design techniques related to solid-state devices in the following general areas:

- Solid-state memory, storage, and logic elements, such as twistors, thin-film memories and associated circuits, photoelectronic circuitry, etc.
- Solid-state microwave amplifying mechanisms, such as parametric amplifiers and masers.
- Solid-state devices performing an integrated circuit function.
- Cryogenic digital and linear applications.
- Novel types of solid-state devices in unique modes of operation such as those utilizing the Hall effect, high-temperature circuit elements, and solid-state filters and delay lines.
- Advanced circuitry with emphasis on significant developments in the art, to the exclusion of data on equipment design.

Papers representing original contributions in these and related fields are invited. An abstract highlighting the nature of the contribution, its significance in the art, and theoretical and experimental results, 300 to 500 words in length, possibly accompanied by key illustrations, plus a 50-word summary for advance program mailings, should be submitted in double-spaced typewritten form (and in triplicate) on or before October 14, 1960, to the program chairman:

Jerome J. Suran
Building 3, Room 115, General Electric Co.
Electronics Park, Syracuse, N. Y.

The abstracts and summary should be accompanied by the author's name, company affiliation, position title, business and home address, telephone contact, and brief biographical sketch.

Members of the 1961 conference committee include:

Chairman: T. R. Finch, Bell Telephone Labs., Murray Hill, N. J.
Secretary: F. H. Blecher, Bell Telephone Labs., Murray Hill, N. J.
Public Relations: Lewis Winner, 152 West 42nd Street, New York 36, N. Y.

HFE SPECIAL ISSUE

The IRE TRANSACTIONS ON HUMAN FACTORS IN ELECTRONICS is planning to devote its March 1961 issue to the topic, "Automation of Human Functions," and manuscripts for that issue are hereby solicited. "Automation of Human Functions" is to be understood as including all techniques whereby the load on the human operator of electronic systems may be lessened through increased automation of his task. Automatic pattern recognition, problem solving, and decision making are examples of subjects included in this topic. Papers need not make original contributions but may review material already published. To be considered, manuscripts must be received by October 15, 1960 and must comply with IRE standards. Manuscripts should be mailed to the guest editor: Dr. Thomas Marill, Bolt Beranek and Newman Inc., 50 Moulton Street, Cambridge 38, Mass.

ELECTRONIC COMPONENTS SPECIAL ISSUE OF PROCEEDINGS OF THE IRE

The IRE Professional Group on Component Parts is sponsoring a special component parts issue of the PROCEEDINGS OF THE IRE which will appear in May of 1961. The theme of the issue is "Electronic Components—Present and Future." The new and most advanced aspects of the current electronic component art will be covered and important trends will be analyzed with regard to their reliability to fulfill equipment and system needs of the future. You are invited to submit manuscripts in keepi with this objective. The following are son suggested fields of interest.

- Discrete components, R, L, C, etc.
  - linear and non-linear
- Functionally complex components
  - integrated
  - film type
  - solid state
- Thin-film components
  - magnetic
  - conductive
  - dielectric
  - semiconductor
- Component-system integration
- Component reliability
- Semiconductors, as applied to electron components
- Electromechanical devices and concepts
- Microwave components
- Ferroelectric and Ferromagnetic devic
- Square-hysteresis-loop components
- Thermoelectric power and devices
- Magneto-optics
- Cryotrons and cryogenics
- Electroluminescence
- Memory devices
- Electronic materials
- Processes, techniques, and analytical tools
  - electron beam machining
  - ultra vacuum techniques
  - microfilms
- Filter and delay lines
  - electronic
  - electromechanical
  - electrostrictive
- Switching devices
  - mechanical
  - solid-state

Manuscripts of papers are due by No ember 1, 1960. Please submit (3) copies the undersigned. One set of the illustratio must be in reproducible form. Photograp and biographies of authors should be i cluded.

Vincent J. Kublin, Chairman
Components Issue Committee
SIGFM/EL-PE
U. S. Army Signal R&D Lab.
Fort Monmouth, N. J.

INTERNATIONAL CONFERENCE O MACHINE TRANSLATION OF LANGUAGES AND APPLIED LANGUAGE ANALYSIS

The Autonomics Division of the Nation Physical Laboratory announces the co vening of an international conference Machine Translation of Languages an Applied Language Analysis, to be he September 5–8, 1961, at the Laborator Teddington, Middlesex, England,

Written contributions to the conferen are invited from workers engaged direct in research into the machine translation natural languages and also from those wh are concerned with the syntactic or semant analysis of languages, where such analys may be of help in achieving machine tran lation.

Papers should be sent to the Chairma of the papers subcommittee of the appr priate area, depending on the country

gin of authors, to be received by him by nuary 31, 1961.

SR, Eastern Europe. . . To be arranged

A. . . . . Professor L. Dostert
Georgetown University
1715 Massachusetts Avenue
Washington 6, D. C., U.S.A.

other countries. . . . . Dr. A. M. Uttley,
Superintendent
Autonomics Div.
National Physical Lab.
Teddington, Middlesex
England

x copies with six abstracts of each paper ould be sent and should be typewritten ith double-spacing, on one side of quarto eets, and must be in one of the official nguages of the Conference, *viz.*, English, ussian or French. In the texts of papers, ly Roman and Cyrillic characters and andard-font symbols should be used, any her characters being put into tables and ferred to from text. Illustration should be line drawing only, on separate sheets d using Indian ink.

The Conference will take place in the w NPL Conference Center, which has a ain hall to seat 400 with provision for lay of simultaneous translations of proedings. There are two smaller conference oms and ample restaurant facilities. Details of the Conference program and of arngements for registration of delegates will announced in the Spring of 1961. The utonomics Division will be pleased to acpt requests for these details at any time.

MISCELLANEOUS

NSF INVITES DOCUMENTATION RESEARCH PROPOSALS

The National Science Foundation has nnounced it will consider proposals during ne current fiscal year for additional research rojects or studies of a fundamental or genral nature that may produce new insights, nowledge, or techniques applicable to cientific information systems and services. Although the Foundation will consider any proposal for a project that may contribute to the general goal of improving the handling of scientific information, the following research areas are of the greatest interest at present:

Information needs of the scientific community. Studies or experiments to provide better understanding of scientific communication processes, scientists' information needs, and the extent to which needs are met by existing publications and information services, or could be met by proposed new types of publications and services.

Information storage and retrieval. Research on the systematization and mechanization of procedures for handling large volumes of scientific information, including procedures for automatic analysis of texts of documents, automatic indexing and abstracting, and automatic searching of stored materials; and tests and evaluations of existing, newly developed, and proposed procedures for handling scientific information.

Mechanical translation. New groups wishing to undertake research on mechanical translation procedures and related studies of language should give first consideration to building upon and complementing the intensive work already accomplished by established groups.

(The semiannual report *Current Research and Development in Scientific Documentation*, available from the Foundation, describes these projects in the U. S. and abroad.)

Address inquiries and proposals to: Documentation Research Program, Office of Science Information Service, National Science Foundation, Washington 25, D. C.

WORKING GROUP FOR BETTER EDUCATION

"The quality of education in elementary and secondary schools is one of the most important factors bearing on the training of young people for doing good work in mathematics, science, and computing machinery." So begins the invitation from Ed Berkeley, Secretary of WGBE, the Working Group for Better Education, and also Chairman of the ACM Secondary Education Committee.

The invitation continues: "I am eager to discover all of you who are interested in and concerned about the quality of education in reading, writing, arithmetic, mathematics, science, and related subjects—the quality of education actually being produced in the schools in your neighborhoods. With 30 to 50 per cent of our young people entering college unable to read adequately for college work, our concern must reach beyond the territory of just mathematics, science, and automatic computers, into the entire junior and senior years of high school.

"We are forming a 'Working Group for Better Education'. We plan to put together and distribute a list of names and addresses of all persons interested in this field; to set up in this group close contact between all members; to exchange information and discussion; and if feasible, to arrange local meetings."

If you are interested in participating in the group, or have comments or suggestions related to the subject of better education, write to Edmund C. Berkeley, Berkeley Enterprises, 815 Washington St., Newtonville, Mass.

Over 450 have already joined WGBE, and about six projects are currently under way, including efforts on teaching machines, use of community resources, and regional problems.

INFORMATION FOR AUTHORS

IRE TRANSACTIONS ON ELECTRONIC COMPUTERS is published quarterly, in March, June, September, and December, with a distribution of over 9000 copies, largely to engineers, logicians, and supervisors in the computer field. Its scope includes the design, theory, and practice of electronic computers and data-processing machines, digital and analog, and parts of certain related disciplines such as switching theory and pulse circuits.

If a paper of widespread interest beyond the computer field is submitted, it will be recommended to the Editor of PROCEEDINGS OF THE IRE for publication. If our reviewers feel that a paper should be submitted to a different IRE TRANSACTIONS, we will so recommend to the author.

Publication time in IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, from receipt of the original manuscript to mailing of the issue, is normally in excess of 5 months, but can be made as little as $3\frac{1}{2}$ months if the occasion demands and the manuscript is carefully prepared.

To avoid delay, please be guided by the following suggestions:

A. Process for Submission of a Technical Paper

1) Send to the Editor three copies of your manuscript, each copy complete with illustrations. (For Letters to the Editor, two copies will do.)

2) Enclose originals for the illustrations, in the style described below. Alternatively, be ready to send the originals immediately upon acceptance of the paper.

3) Enclose a separate sheet giving your preferred address for correspondence and return of proofs.

4) Enclose a technical biography and photograph of each author, or be ready to supply these upon acceptance of the paper. For biography style, see any IRE journal.

5) If the manuscript has been presented, published, or submitted for publication elsewhere, please so inform the Editor. Our primary objective is to publish technical material not available elsewhere, but on occasion we publish papers of unusual merit that have appeared or will appear before other audiences.

B. Style for Manuscript

1) Typewrite, double or $1\frac{1}{2}$ space; use one side of sheet only. (Good office-duplicated copies are acceptable.)

2) Provide an informative 100- to 250-word summary (abstract) at the head of the manuscript. It will appear with the paper and also separately in PROCEEDINGS OF THE IRE.

3) Provide a separate double-spaced sheet listing all footnotes, beginning with "*Received by the PGEC _____," and "†(Affiliation of author)," and continuing with numbered references. Acknowledgment of financial support is often placed at the end of the asterisk footnote.

4) References may appear as numbered footnotes, or in a separate bibliography at the end of the paper, with items referred to by numerals in square brackets, e.g., [12]. In either case, references should be complete, and in IRE style.

Style for papers: Author (with initials first), title, journal title, volume number, inclusive page numbers; month, year.

Style for books: Author, title, publisher, location, year; page or chapter numbers (if desired).

See this or previous issues for further examples.

5) Provide a separate sheet listing all figure captions, in proper style for the typesetter, *e.g.*: "Fig. 1—Example of a disjoint and distraught manifold."

C. Style for Illustrations

1) Originals for illustrations should be sharp, noise-free, and of good contrast. We regret that we cannot provide drafting or art service.

2) Line drawings should be in India ink on drafting cloth, paper, or board. Use $8\frac{1}{2} \times 11$ inch size sheets if possible, to simplify handling of the manuscript.

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